

Converting AXI to Avalon interfaces

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V 1.0

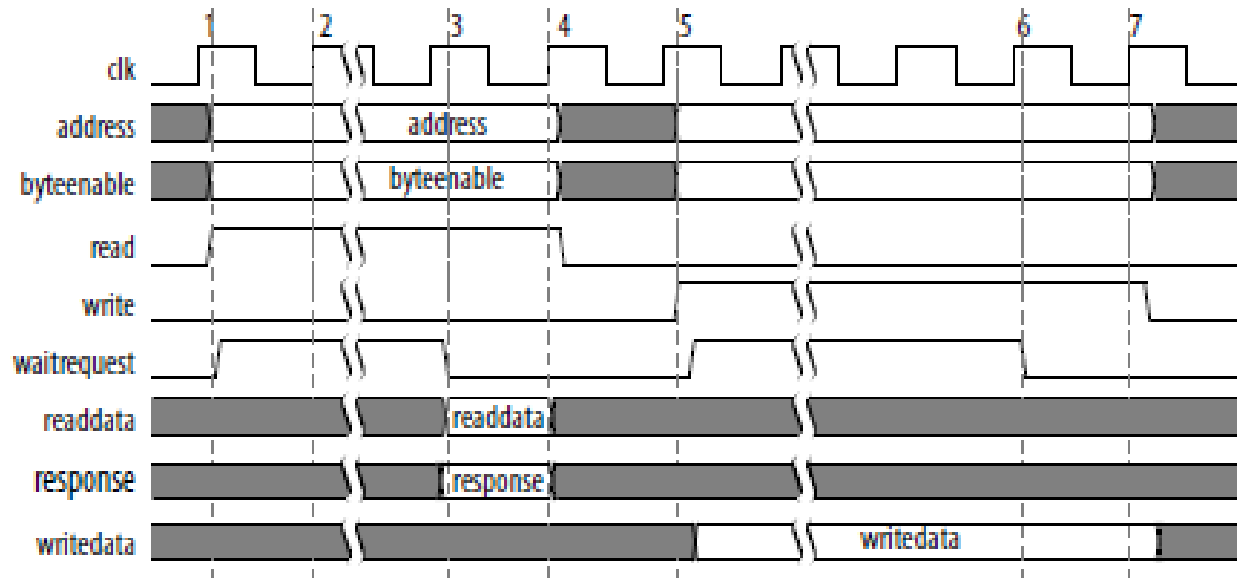
This presentation shows how to interface Avalon interfaces with AXI interfaces

- AXI Lite MM to Avalon MM
- AXI Stream to Avalon ST

References : Avalon Interface Specification and AMBA AXI protocol specification

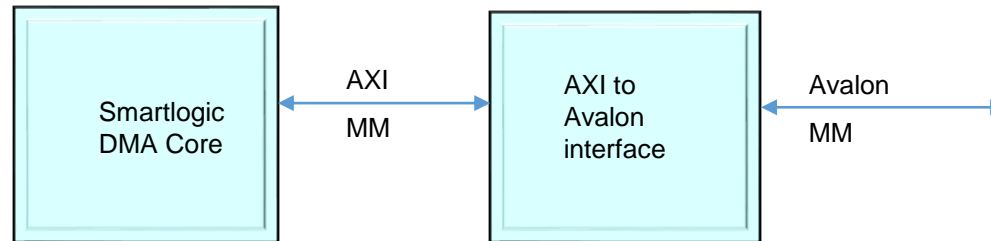
The Avalon Interface specification defines the Avalon MM behavior:

Read and Write Transfers with Waitrequest



The shown case is with `waitRequestAllowance = 1`

Major differences between Avalon and AXI is, that AXI allows to issue read and write requests in parallel, whereas Avalon MM allows only one request of one type per time.



In order to interface from AXI MM to Avalon MM interface standards, Smartlogic provides a AXI to Avalon interface block. The module is called `axi_mm_avalon_mm_bridge.vhd`. This module connects to the AXI MM (`m<nn>_axi_*`) signals and provides a Avalon MM interface.

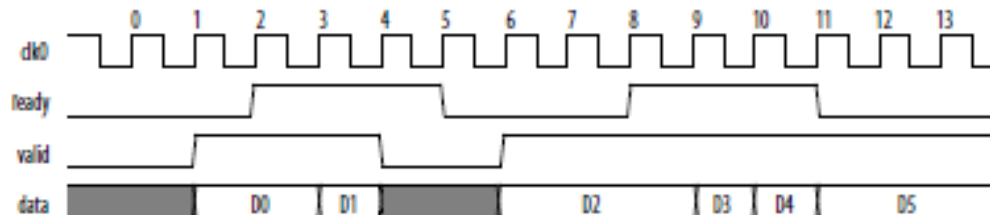
The Avalon Interface specification defines the Avalon Stream behavior:

readyLatency = 0, readyAllowance = 0

When `readyLatency = 0` and `readyAllowance = 0` the source can assert `valid` at any time. The sink captures the data from source only when `ready = 1`.

The following figure demonstrates these events:

1. In cycle 1 the source provides data and asserts `valid`.
2. In cycle 2, the sink asserts `ready` and D0 transfers.
3. In cycle 3, D1 transfers.
4. In cycle 4, the sink asserts `ready`, but the source does not drive valid data.
5. The source provides data and asserts `valid` on cycle 6.
6. In cycle 8, the sink asserts `ready`, so D2 transfers.
7. D3 transfers at cycle 9 and D4 transfers at cycle 10.



The shown case with `readyLatency = 0` and `readyAllowance = 0` is identical with AXI Stream.

Signal translation table :

Avalon Stream	AXI Stream
ready	s<nn>_axis_tready
valid	s<nn>_axis_tvalid
data	s<nn>_axis_tdata
clk	s<nn>_axis_aclk
startofpacket	s<nn>_axis_tuser(0)
endofpacket	s<nn>_axis_tuser(1)

No additional logic is required to interface Avalon ST with AXI stream.
Remember to configure your Avalon interface with readyLatency = 0 and readyAllowance = 0 !