DATASHEET

PCIe Multi-Function Option for DMA IP Cores

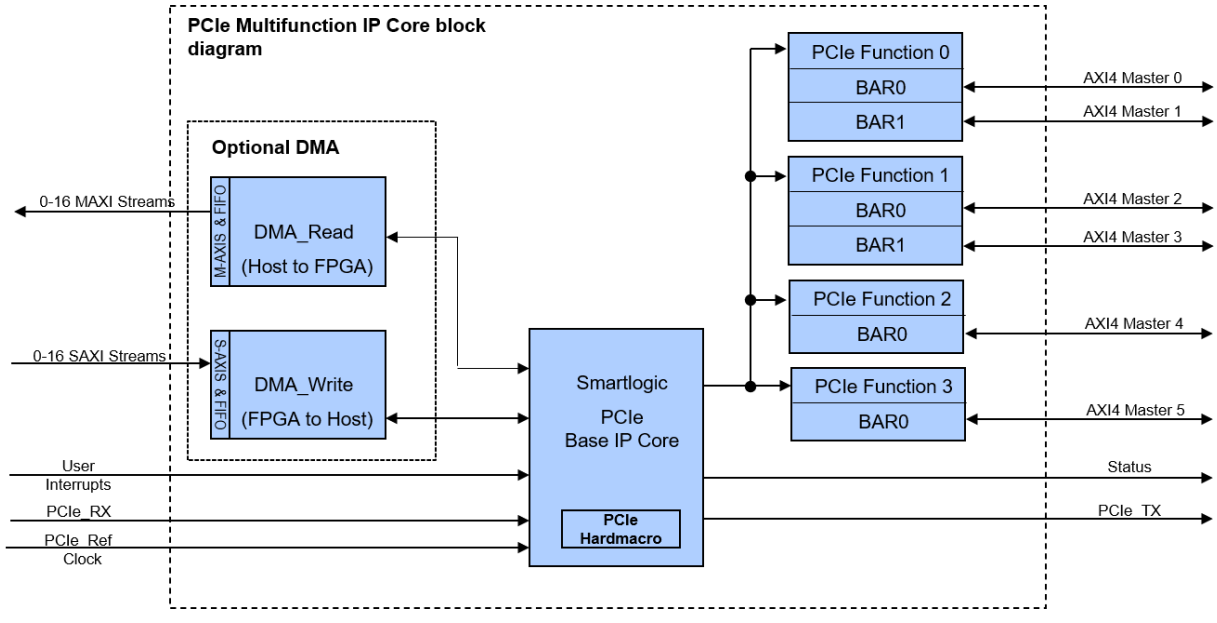
Product Overview

The PCI Express specification allows endpoints that incorporate several physical PCIe functions that share the same PCIe connection. Such endpoints are called multi-function devices. The big advantage of a multi-function device is, that a separate device driver can be associated to each physical function. This simplifies driver development and maintenance significantly by separating the peripheral functions logically into different device drivers.
Most FPGA families support multi-function devices but only on a very low level.
This product offers a full-blown multi-function IP core solution with optional DMA support based on our High Channel Count (HCC) IP Core. The core operates with industry standard interfaces (AXI and AXI Stream) and encapsulates the whole PCI Express protocol know-how. This frees the FPGA designer to concentrate on the project specific design tasks.

IP Features

- Multi-function support with up to 8 PCIe functions.
- Up to 8 AXI Masters to interface user registers
- Up to 16 AXI Stream Slave interfaces
- Up to 16 AXI Stream Master interfaces
- User transmits / receives only user data without PCIe protocol knowledge
- Supports 32-Bit and 64-Bit addressing
- Independent clocking and data width for each AXI Stream interface
- Adjustable priority control
- Memory size up to 4 GByte per streaming channel
- Based on AMD / Altera integrated PCI-Sig compliant PCIe Block (HardIP)
- Link speed Gen 1-4, link widths x1-x8 (depends on the capabilities of the device)
- Available for all AMD and Altera devices

Block Diagram – Example Configuration



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The example shows 4 of the 8 available PCIe functions and how the BARs of each function can be mapped to AXI masters. The user has full control at compile time to map up to 8 AXI masters to the active PCIe functions. Unused AXI4 masters do not occupy logic resources.

DMA is available and can be shared over the implemented functions.

Supported number of PCIe functions

The following table lists the number of supported PCIe functions for each FPGA device family:

FPGA Device	max PCIe functions	Link width
Artix 7, Kintex 7	6*	Only X1 supported
Cyclone 5, Arria 5	8	All link widths supported
Ultrascale	2	
Ultrascale+ (Artix, Kintex, Virtex, Spartan)	4	
Arria 10	0**	
Stratix 10 H-Tile	4	

* 7 Series supports multi-function with our patented multi-function extension that extends the existing HardIP with up to 6 functions.
** Arria 10 HIP does not support multi-function

FPGA Resource Utilization

The following table lists different example configurations and the required FPGA resources:

FPGA Device	AMD Configuration	LUTs	FFs	BRAM
Artix 7, Kintex 7	2 Functions, 2 AXI Masters	3,151	3,436	8
Ultrascale+	4 Functions, 4 AXI Masters	3,603	8,123	24
	Altera Configuration	ALMs	FFs	BRAM
Cyclone V Arria V	4 Functions, 4 AXI Masters	2,507	4,354	2

These numbers include the resources of the PCIe Hard-IP. In case DMA is required, add the resources of the HCC Core to the numbers, see HCC Core datasheet for details.

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Deliverables

- Encrypted VHDL or source code for easy design flow integration
- Comprehensive user guide and application notes
- Reference design
- Windows / Linux driver package (option)
- PCIe test bench with high-speed simulation mode
- Technical support

Evaluation

This IP Core can be evaluated as an encrypted version. Request a free 30-day evaluation license for ISIM, Modelsim or Aldec simulators at:

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Smartlogic is a member of the Altera Partner Alliance and AMD's Alliance Program.

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