DATASHEET

High Channel Count DMA IP Core for PCIe

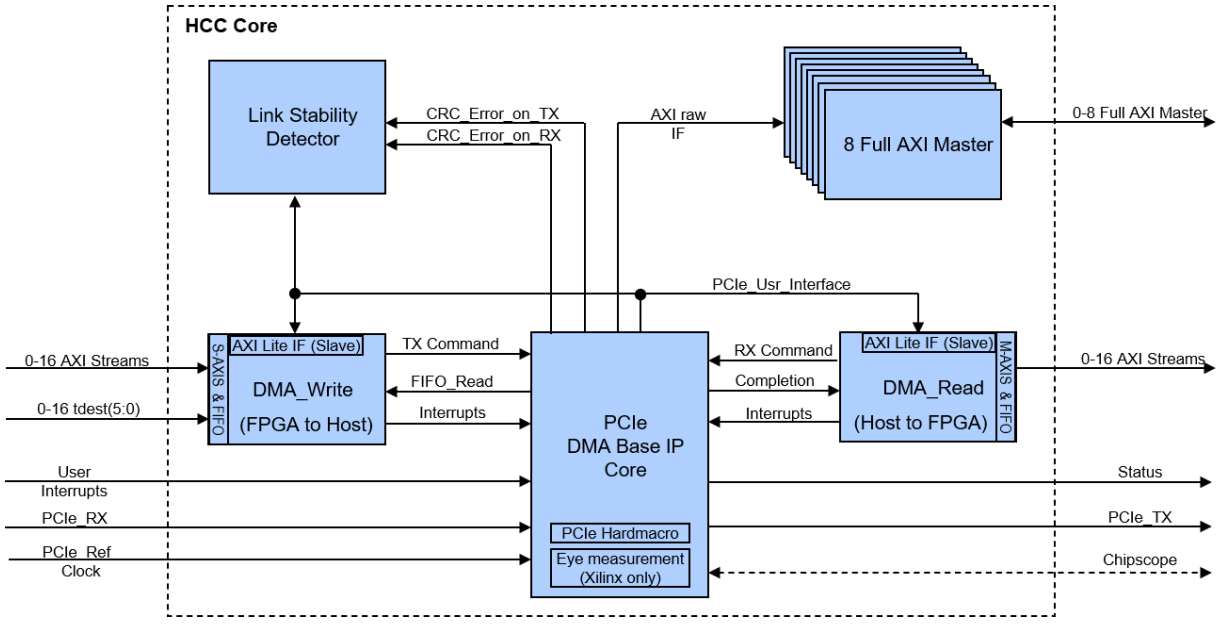
Product Overview

The High Channel Count (HCC) DMA IP core for PCI-Express is a powerful PCIe Endpoint with multiple industry standard AXI Interfaces. This IP addresses continuous streaming applications from up to 64 different data sources. Each channel is able to transmit data into a separate memory area. Up to 16 AXI Stream masters read DMA Data from the host and present it to the user logic. Additional 8 AXI4 masters are available to interface full AXI or AXI-Lite peripherals with the host.
Due to a powerful arbitration scheme, it is possible to control the priority of each DMA channel over other active channels.
The link stability detector module measures the signal integrity of the PCI Express Link for lab or production tests to prevent shipments of faulty devices (Xilinx only).
This IP core enables the developer to build complex PCI Express endpoints with no specific PCI Express protocol know how. The user only transmits or receives payload data and does not have to assemble valid PCI Express packets.

IP Features

- Multi-channel architecture
- Non-blocking approach, an incomplete AXI Stream packet does not block other AXI Streams
- Up to 16 AXI Stream Slave interfaces with up to 64 channels addressable via TDEST
- Up to 16 AXI Stream Master interfaces
- Up to 8 AXI Masters to interface user registers
- User transmits / receives only user data without PCIe protocol knowledge
- Supports 32-Bit and 64-Bit addressing
- Independent clocking and data width for each AXI Stream interface
- Configurable priority control of each AXI Stream
- Adjustable priority control
- Memory size up to 4 GByte per streaming channel
- Based on Xilinx / Intel integrated PCI-Sig compliant PCIe Block (HardIP)
- Link speed Gen 1-4, link widths x1-x8
- Multi-function supported as an option
- Available for all Xilinx and Intel devices

Block Diagram



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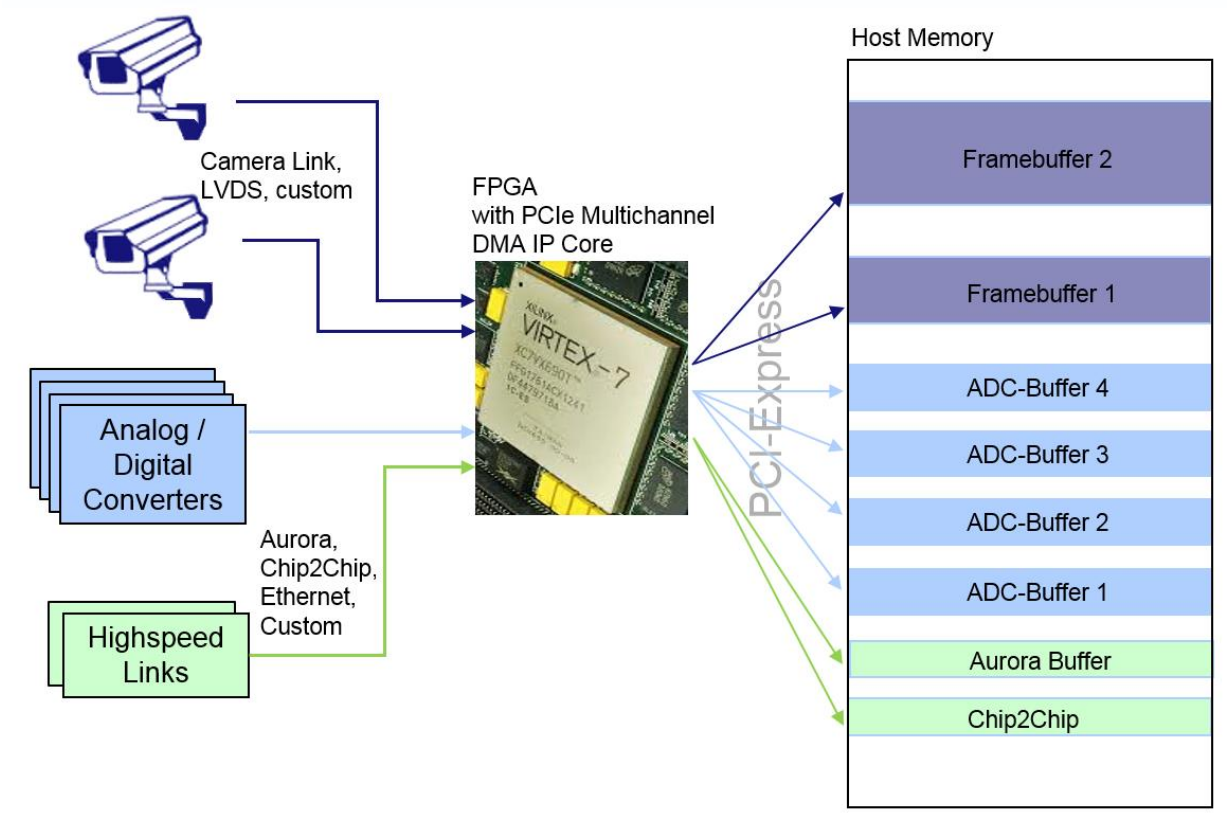
IP Application Example: “Data Streaming”

Due to its generic architecture, the multi-channel HCC DMA IP Core for PCI Express fits into many applications. The following diagram shows typical streaming applications, where data streams have to be sent ordered to the host memory:



Typical streaming data sources are:

Video cameras, high-speed Analog-Digital-Converter samples, high-speed links like Aurora, Ethernet or others.

Up to 64 independent streaming sources with a dedicated target buffer are supported.

Each data interface can operate at its own clock domain and its own data width (8, 16, 32, 64, 128 or 256 Bit).

The target can be either the host memory or any other PCI Express endpoint in the system.

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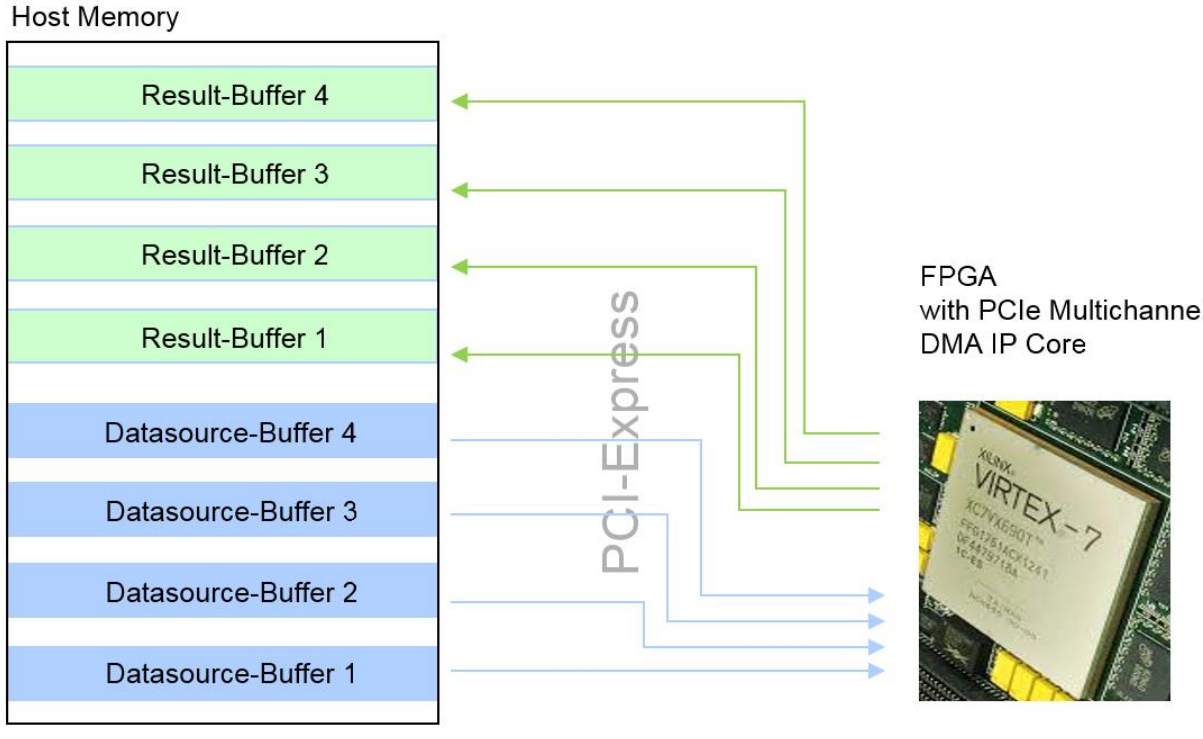
IP Application “Coprocessor”

Another well-known application is the custom data Coprocessor within a FPGA. The data which has to be processed is either fetched via DMA Read Requests from the FPGA or served from the CPU or another PCI Express endpoint. The processed results will be written back into separate memory buffers by using DMA Write requests. Application examples are data encryption and video data processing.



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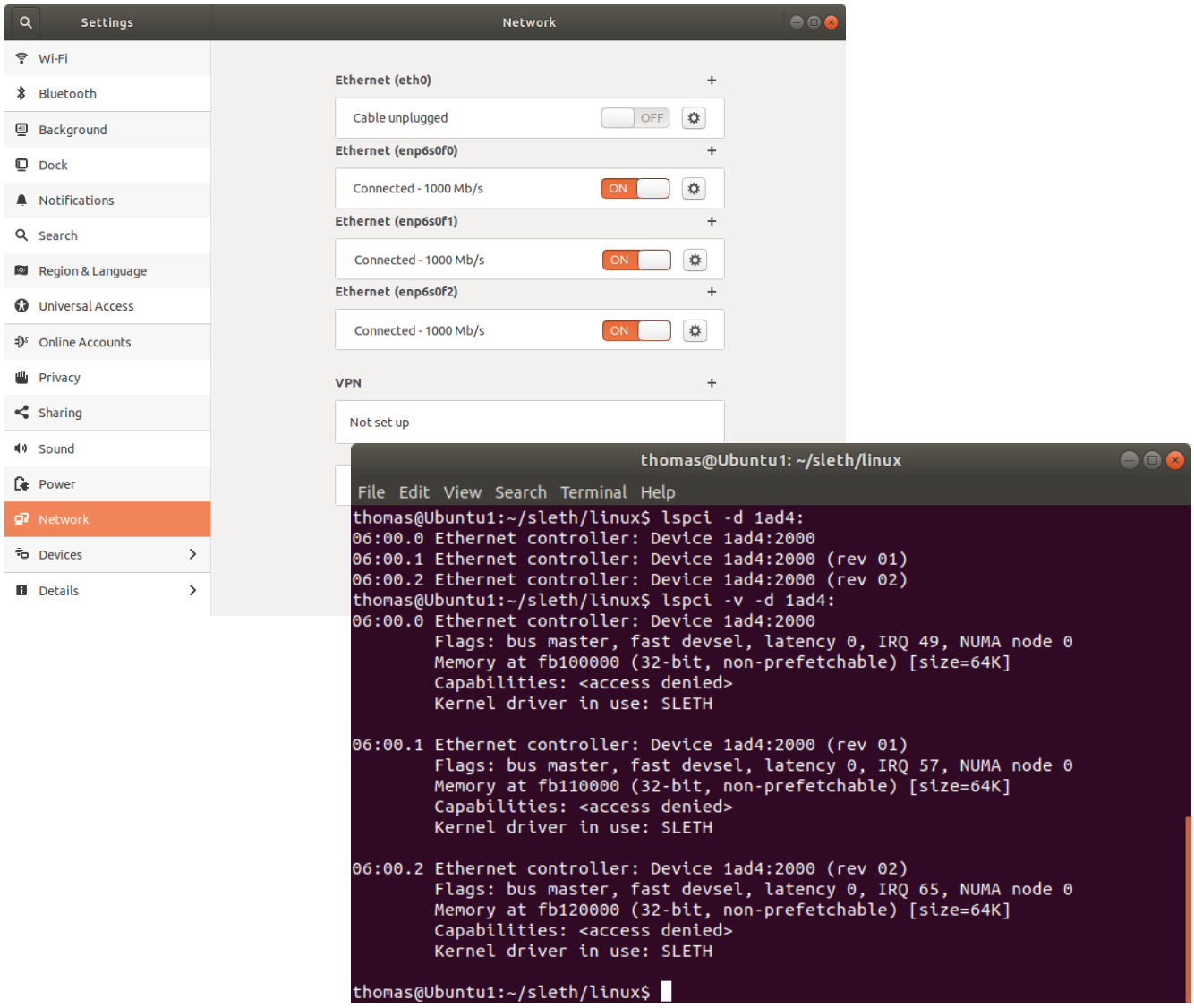
IP Application “Ethernet NIC”

The HCC IP core allows to add additional ethernet links to the host via PCI Express. Ethernet link speed is at your choice and limited only by the PCIe bandwidth. The Smartlogic device driver integrates these new links into Linux in order to allow access to the user.

In conjunction with the PCIe multi-function option it is possible to connect up to 8 ethernet links that share the same PCIe connection to the FPGA. The exact number of ethernet links depends on the multi-function capabilities of the PCIe HardIP block of the FPGA. Check with your FPGA vendor if multi-function is supported and how many physical functions are available for PCI Express.

This example shows 3 additional ethernet links on a Cyclone 5 device and how they appear on Linux:



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FPGA Resource Utilization

The following table lists different example configurations and the required FPGA resources:

FPGA Device	Xilinx Configuration	LUTs	LUTR	FFs	BRAM
Artix 7 Kintex 7	64-bit Architecture, 32 DMA Write Channels, 1 Master, 0 Read Channels	3,577	632	3,418	3
7 Series, Ultrascale Ultrascale+	256-bit Architecture, 9 DMA Write, 1 Master, 8 Read interfaces	11,156	1,835	13,321	22
	Intel Configuration	ALMs		FFs	BRAM
Cyclone 5, Arria 5 / 10, Stratix 10	256-bit Architecture, 64 DMA Write Channels, 1 AXI Master, 2 Read Channels	10,373		13,562	81
Cyclone 5, Arria 5 / 10, Stratix 10	256-bit Architecture, 9 DMA Write, 1 Master, 8 Read interfaces	18,204	3,510	25,077	129

These numbers include the resources of the PCIe Hard-IP and the resources for the AXI Stream FIFOs for each configured channel.
LUTR are distributed RAM cells. The user can choose between BlockRAM or LUT RAM implementation style.

Deliverables

- Encrypted VHDL or source code for easy design flow integration
- Comprehensive user guide and application notes
- Reference design
- Windows / Linux driver package (option)
- PCIe test bench with high-speed simulation mode
- Technical support

Evaluation

This IP Core can be evaluated as an encrypted version. Request a free 30-day evaluation license for ISIM, Modelsim or Aldec simulators at:

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Smartlogic is a member of the Intel Partner Alliance and Xilinx's Alliance Program.

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