

High Channel Count DMA IP Core for PCIe

Product Overview

The High Channel Count (HCC) DMA IP core for PCI-Express is a powerful PCIe Endpoint with multiple industry standard AXI Interfaces. This IP addresses continuous streaming applications from up to 64 different data sources. Each channel is able to transmit data into a separate memory area. Up to 16 AXI Stream masters read DMA Data from the host and present it to the user logic. Additional 8 AXI4 masters are available to interface full AXI or AXI-Lite peripherals with the host.

Due to a powerful arbitration scheme, it is possible to control the priority of each DMA channel over other active channels.

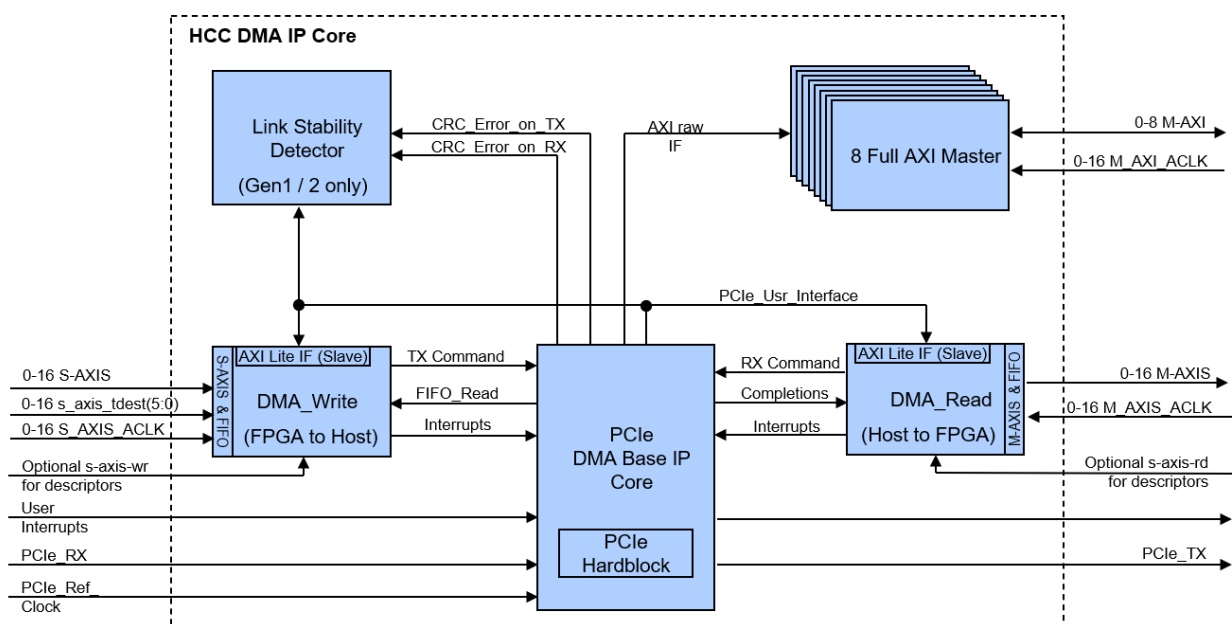
All interfaces support fully parallel operation without any interferences. Interfaces that are not required can be turned off individually and do not occupy logic resources.

This IP core enables the developer to build complex PCI Express endpoints with no specific PCI Express protocol know how. The user only transmits or receives payload data and does not have to assemble valid PCI Express packets.

IP Features

- Lowest logic resource count in the industry, fits into very small FPGA devices
- Easy timing closure for Lattice Gen3-X4
- Multi-channel architecture
- Continuous high throughput data streaming
- Non-blocking approach, an incomplete AXI Stream packet does not block other AXI Streams
- Up to 16 AXI Stream Slave interfaces with up to 64 channels addressable via TDEST
- Up to 16 AXI Stream Master interfaces
- Up to 8 AXI Masters to interface user registers
- User transmits / receives only user data without PCIe protocol knowledge
- Independent clocking and data width for each AXI Stream interface
- Optional streaming interfaces for descriptors provided from the FPGA fabric
- Based on AMD / Altera / Lattice integrated PCI-Sig compliant PCIe Block (HardIP)
- Link speed Gen 1-4, link widths x1-x8
- Available for most AMD, Altera and Lattice devices

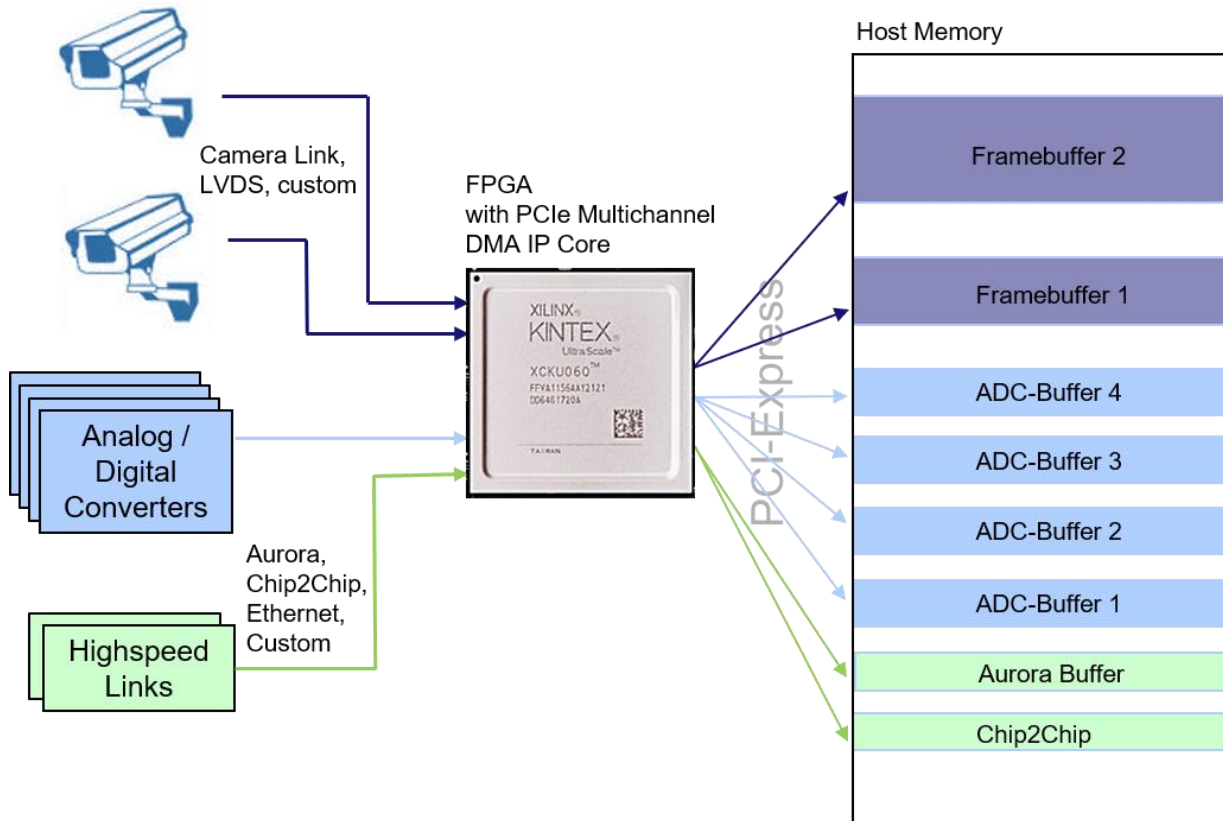
Block Diagram



Contact

IP Application Example: "Data Streaming"

Due to its generic architecture, the multi-channel HCC DMA IP Core for PCI Express fits into many applications. The following diagram shows typical streaming applications, where data streams have to be sent ordered to the host memory:



Typical streaming data sources are:

Video cameras, high-speed Analog-Digital-Converter samples, high-speed links like Aurora, Ethernet or others.

Up to 64 independent streaming sources with a dedicated target buffer are supported.

Each data interface can operate at its own clock domain and its own data width (8, 16, 32, 64, 128 or 256 Bit).

The target can be either the host memory or any other PCI Express endpoint in the system.

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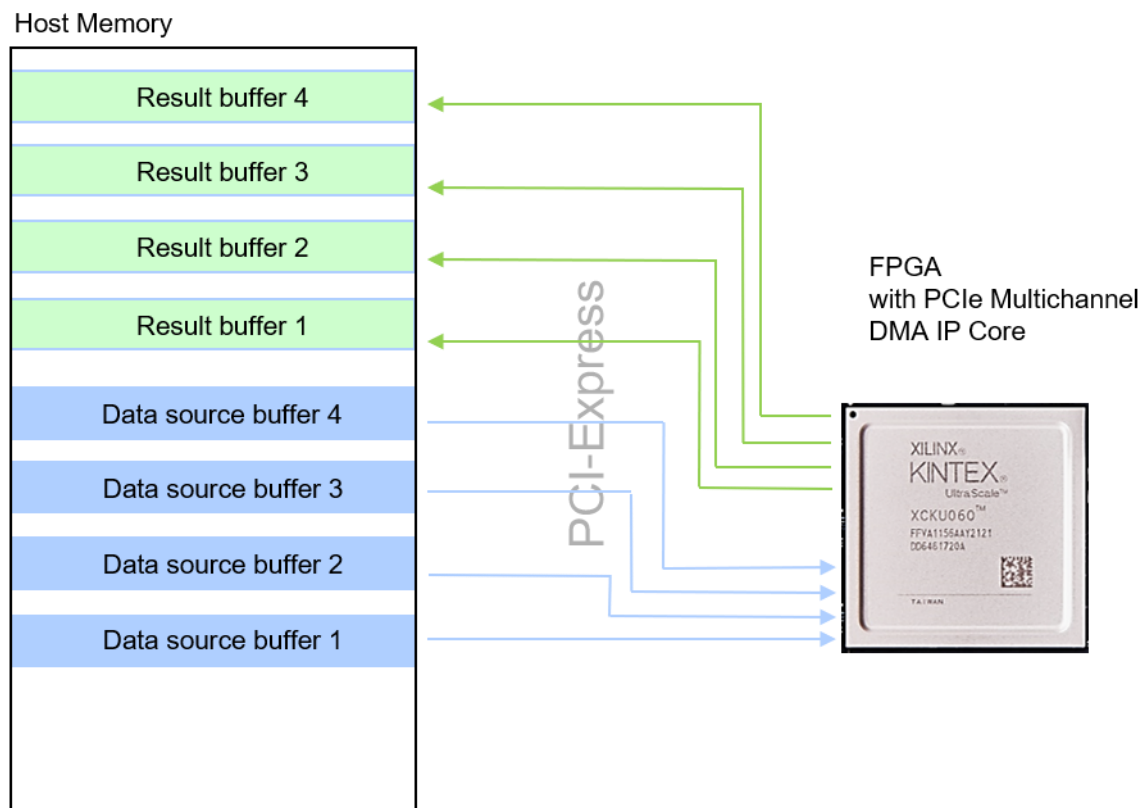
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IP Application “Coproprocessor”

Another well-known application is the custom data Coprocessor within a FPGA. The data which has to be processed is either fetched via DMA Read Requests from the FPGA or served from the CPU or another PCI Express endpoint. The processed results will be written back into separate memory buffers by using DMA Write requests. Application examples are data encryption and video data processing.



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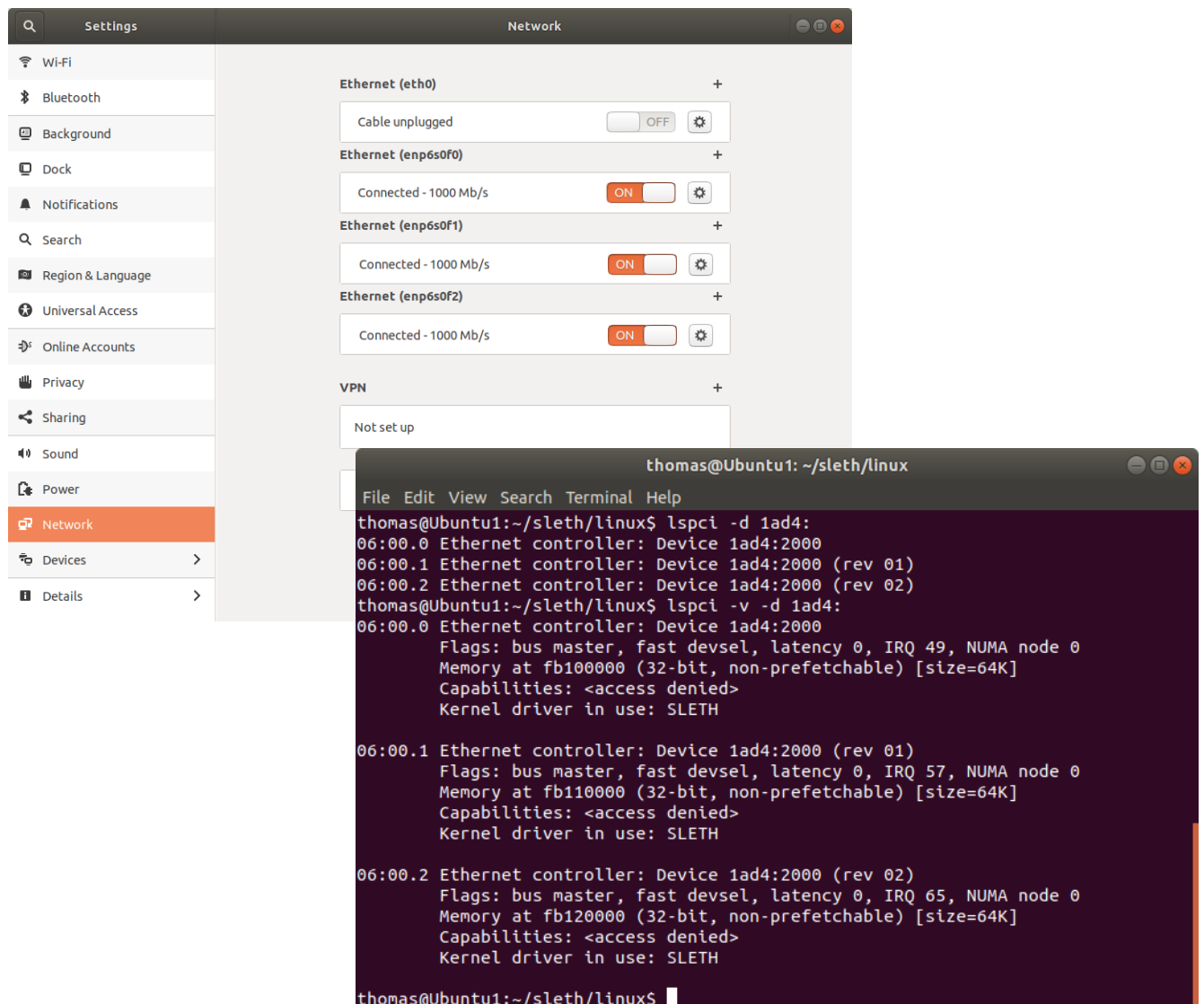
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IP Application “Ethernet NIC”

The HCC IP core allows to add additional ethernet links to the host via PCI Express. Ethernet link speed is at your choice and limited only by the PCIe bandwidth. The Smartlogic device driver integrates these new links into Linux in order to allow access to the user.

In conjunction with the PCIe multi-function option it is possible to connect up to 8 ethernet links that share the same PCIe connection to the FPGA. The exact number of ethernet links depends on the multi-function capabilities of the PCIe HardIP block of the FPGA. Check with your FPGA vendor if multi-function is supported and how many physical functions are available for PCI Express.

This example shows 3 additional ethernet links on a Cyclone 5 device and how they appear on Linux:



The image shows a Linux desktop environment with the 'Settings' application open to the 'Network' section. On the left, a sidebar lists various system settings, with 'Network' highlighted. The main window displays the network configuration for three additional ethernet interfaces: 'Ethernet (eth0)', 'Ethernet (enp6s0f0)', and 'Ethernet (enp6s0f1)'. Each interface is shown as 'Connected - 1000 Mb/s' with an 'ON' toggle switch and a gear icon for settings. Below these, the 'VPN' section is shown as 'Not set up'.

Overlaid on the bottom right is a terminal window titled 'thomas@Ubuntu1: ~/sleth/linux'. The terminal shows the following commands and output:

```
thomas@Ubuntu1:~/sleth/linux$ lspci -d 1ad4:
06:00.0 Ethernet controller: Device 1ad4:2000
06:00.1 Ethernet controller: Device 1ad4:2000 (rev 01)
06:00.2 Ethernet controller: Device 1ad4:2000 (rev 02)
thomas@Ubuntu1:~/sleth/linux$ lspci -v -d 1ad4:
06:00.0 Ethernet controller: Device 1ad4:2000
    Flags: bus master, fast devsel, latency 0, IRQ 49, NUMA node 0
    Memory at fb100000 (32-bit, non-prefetchable) [size=64K]
    Capabilities: <access denied>
    Kernel driver in use: SLETH

06:00.1 Ethernet controller: Device 1ad4:2000 (rev 01)
    Flags: bus master, fast devsel, latency 0, IRQ 57, NUMA node 0
    Memory at fb110000 (32-bit, non-prefetchable) [size=64K]
    Capabilities: <access denied>
    Kernel driver in use: SLETH

06:00.2 Ethernet controller: Device 1ad4:2000 (rev 02)
    Flags: bus master, fast devsel, latency 0, IRQ 65, NUMA node 0
    Memory at fb120000 (32-bit, non-prefetchable) [size=64K]
    Capabilities: <access denied>
    Kernel driver in use: SLETH

thomas@Ubuntu1:~/sleth/linux$
```

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FPGA Resource Utilization

The following table lists different example configurations and the required FPGA resources:

AMD Device	Configuration	LUTs	LUTR	FFs	BRAM
Artix 7 Kintex 7	64-bit Architecture, 32 DMA Write Channels (1 s-axis), 0 m-axis, 1 m-axi	3,577	632	3,418	3
7 Series, Ultrascale	256-bit Architecture, 1 s-axis, 0 m-axis, 1 m-axi (low BRAM count)	5,781	752	8,752	10
	256-bit Architecture, 4 s-axis, 4 m-axis, 1 m-axi (high buffering capacity)	12,526	1,182	16,988	58.5
Ultrascale+*	256-bit Architecture, 1 s-axis, 0 m-axis, 1 m-axi (low BRAM count)	6,748		11,680	27
	256-bit Architecture, 4 s-axis, 2 m-axis, 1 m-axi (high buffering capacity)	10,526		16,830	60
Versal with PL_PCIE4	256-bit Architecture, 1 s-axis, 0 m-axis, 1 m-axi (low BRAM count)	5,870	618	11,089	2
	256-bit Architecture, 4 s-axis, 4 m-axis, 1 m-axi (high buffering capacity)	12,799	553	19,411	52
Altera Device	Configuration	ALMs	LUTR	FFs	BRAM
Cyclone 5, Arria 5 / 10, Stratix 10	256-bit Architecture, 64 DMA Write Channels (1 s-axis), 2 m-axis, 1 m-axi	10,373		13,562	81
Cyclone 5, Arria 5 / 10, Stratix 10	256-bit Architecture, 9 s-axis, 8 m-axis, 1 m-axi	18,204	3,510	25,077	129
Lattice Device	Configuration	LUTs	LUTR	FFs	EBR
Crosslink NX Certus NX Certus Pro NX	256-bit Architecture, 1 s-axis, 0 m-axis, 1 m-axi	7,342	1,944	5,990	3
	256-bit Architecture, 4 s-axis, 0 m-axis, 1 m-axi	9,503	3,186	8,292	3
	256-bit Architecture, 4 s-axis, 4 m-axis, 1 m-axi	16,890	7,122	17,097	5

* includes Spartan, Artix, Kintex and Virtex Ultrascale+ Devices

These numbers include the resources of the PCIe Hard-IP and the resources for the AXI Stream FIFOs for each configured channel. LUTR are distributed RAM cells. The user can choose between BlockRAM or LUT RAM implementation style.

**Note : The Lattice Version of the HCC IP Core requires a license to use the PCIe HardIP. This license is not included and must be purchased separately from Lattice.

Deliverables

- Encrypted VHDL or source code
- Comprehensive user guide and app notes
- Reference design
- Windows or Linux driver package
- PCIe test bench with high-speed simulation mode
- Technical support

Evaluation

This IP Core can be evaluated as an encrypted version. Request a free 30-day evaluation license at:

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Smartlogic is a member of the Altera Partner Alliance, AMD's Alliance Program and the Lattice Partner Network.

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