DATASHEET

Multi-Channel AXI DMA Engine

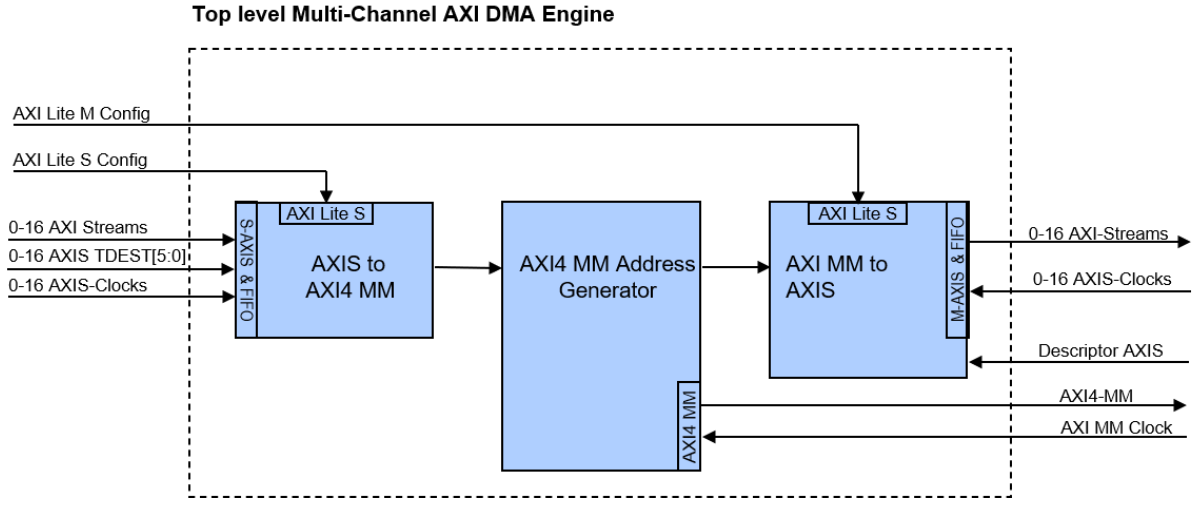
Product Overview

The Multi-Channel AXI DMA engine IP Core for AXI4 is a powerful programmable AXI Stream to AXI memory mapped bridge with sophisticated data addressing options. These features allow data accesses on a tile basis in order to address regions of interest (ROI) based applications like stereo cameras, 2D picture compression algorithms and others.
Up to 16 independent AXI Stream Slaves write DMA data to the connected AXI Slaves. Up to 16 AXI Stream Masters read DMA data from the connected slaves and present it to the user logic. Each channel operates in its own address map. This IP core targets continuous data streaming applications (i.e. data acquisition, Video and DSP applications) with AXI Stream interfaces and is well suited for standard AXI4 Slaves including DDR Memory Interfaces or the Xilinx Zynq™ devices. A sophisticated Linux kernel mode device driver allows easy data access from user mode.

IP Features

- Multi-channel architecture
- Non-blocking approach, an incomplete AXI Stream packet does not block other AXI Streams
- Up to 16 AXI Stream Slave interfaces that can address up to 64 destinations
- Up to 16 AXI Stream Master interfaces
- Independent clocking and data width for each AXI Stream interface
- Configurable via 2 AXI Lite or AXI Stream interfaces
- Linux Kernel Mode Driver included
- Powerful addressing schemes supported: Ascending, descending and streaming into or from regions of interest (ROI)
- Memory size up to 4 GByte per streaming channel
- GStreamer™ compatible
- Available for all Xilinx and Intel devices

Block Diagram



FPGA Resource Utilization

The following table lists different example configurations and the required FPGA resources:

FPGA Device	Configuration	LUTs	LUTR	FFs	BRAM
7 Series	64-bit AXI MM Master, 2 AXI Stream Slaves, 2 AXI Stream Masters	3,577	632	3,418	3
Zync MPSoC	128-bit AXI MM Master, 9 AXI Stream Slaves, 8 AXI Stream Master	11,156	1,835	13,321	22

LUTR are distributed RAM cells. The user can choose between BlockRAM or LUT RAM implementation style.

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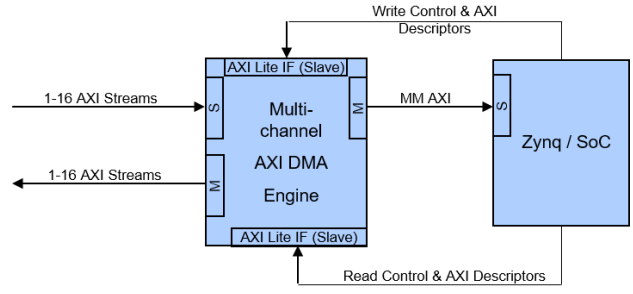
Application Example with a SoC

The Multi-channel AXI DMA engine is typically used with SoC / Zynq based FPGAs where AXI / Avalon data streams like video frames or A/D converter data have to be transferred into the SoC's DDR memory.

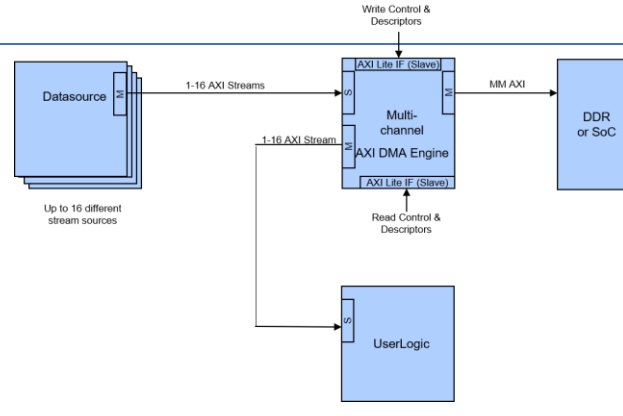
The included Linux Kernel mode device driver with its high-level user mode library allows fast and very easy access to the data. The compatibility of the driver with GStreamer™ provides the user with a very powerful open-source video framework for further processing.



Standalone Application

This IP core can also be used in non-SoC based FPGA designs, for example when a DDR memory is required as a data buffer.

Up to 16 streaming slave interfaces transfer data to the DDR and up to 16 streaming masters move the data out of the DDR memory.



Deliverables

- Encrypted VHDL or source code for easy design flow integration
- Comprehensive user guide
- Reference design
- Test bench
- 1/2 year of technical support included
- Linux device driver with powerful user-mode library

Evaluation

This IP Core can be evaluated as an encrypted version. Request a free 30-day evaluation for ISIM, Modelsim or Aldec simulators at:

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Smartlogic is a member of the Intel Partner Alliance and Xilinx's Alliance Program.

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