DATASHEET

AXI Bridge for PCIe IP Core

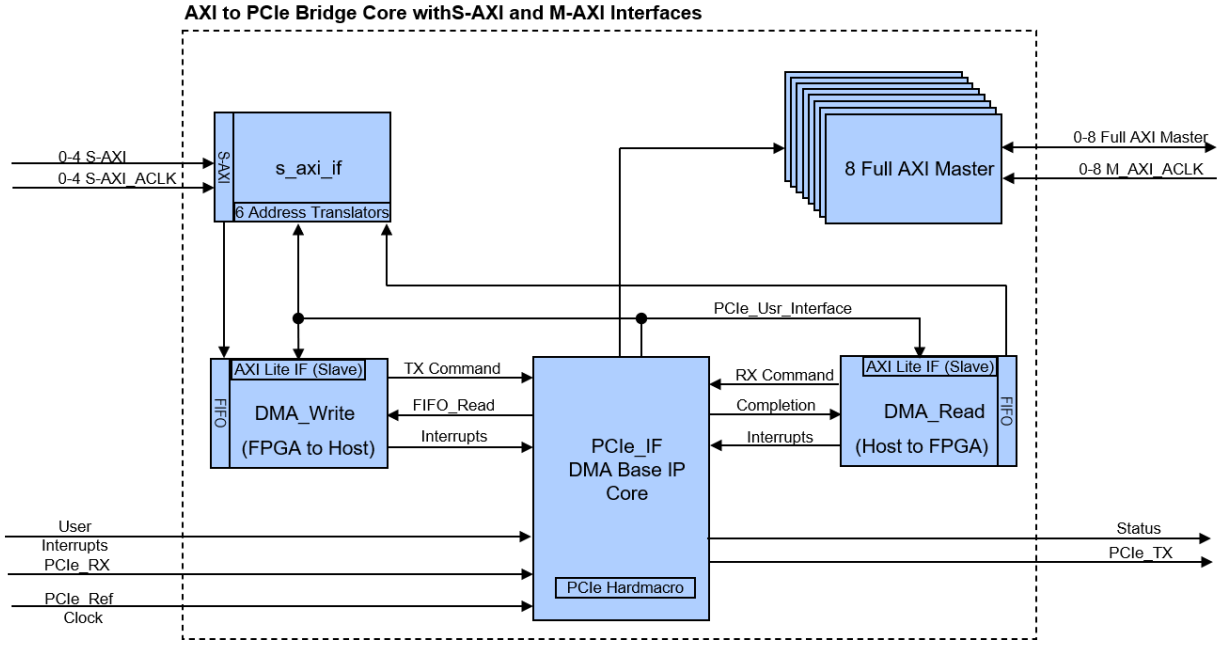
Product Overview

The AXI Bridge for PCIe IP core is Smartlogic's IP solution with a powerful mix of multiple industry standard memory mapped AXI Interfaces.The AXI Bridge IP core translates the AXI4 memory read or writes to PCI-Express Transaction Layer Packets and translates PCIe memory read and write requests to AXI4 transactions.
All interfaces support fully parallel operation without any interferences. Interfaces that are not required can be turned off individually and do not occupy logic resources.
This IP core enables the developer to build complex PCI-Express endpoints with no specific PCI Express protocol know-how. The user only transmits or receives payload data and does not have to assemble valid PCI-Express TLP packets.
A powerful kernel mode device driver is shipped with the IP for Windows and Linux OS to ensure easy software integration of the core.

IP Features

- Up to 4 S-AXI4 interfaces for bridging applications (incl peer to peer applications)
- 6 AXI BARs with dynamic address translators
- Non-blocking approach, an incomplete AXI packet does not block other AXI interfaces
- Up to 8 AXI4 Masters to interface user registers
- User transmits / receives only user data without PCIe protocol knowledge
- Independent clocking and data width for each AXI interface
- Built in completion sorting: S-AXI read requests are answered always in the requested order
- High performance throughput: BVALID is asserted immediately after the end of the packet (WLAST)
- Based on Xilinx / Intel / Lattice integrated PCI-Sig compliant PCIe Block (HardIP)
- Link speed Gen 1-4, link widths x1-x8
- Available for most Xilinx, Intel and Lattice devices

Block Diagram



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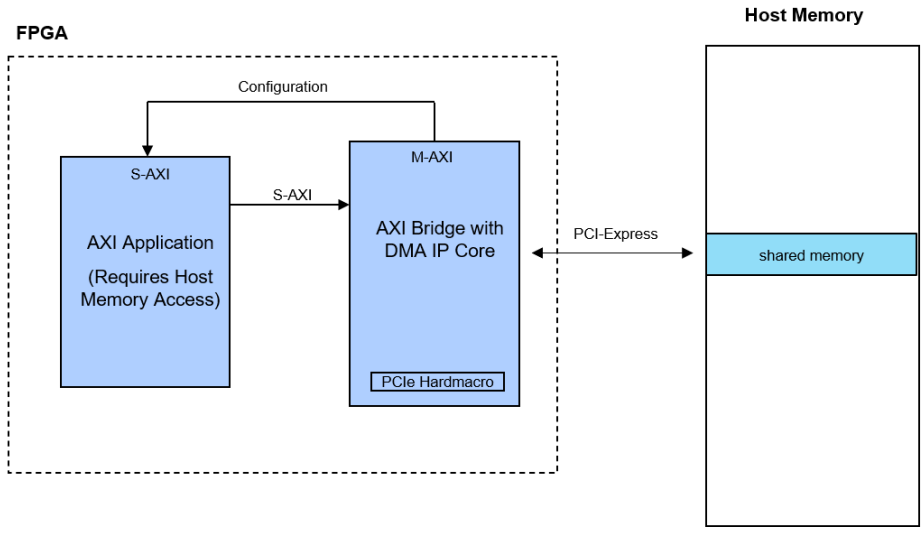
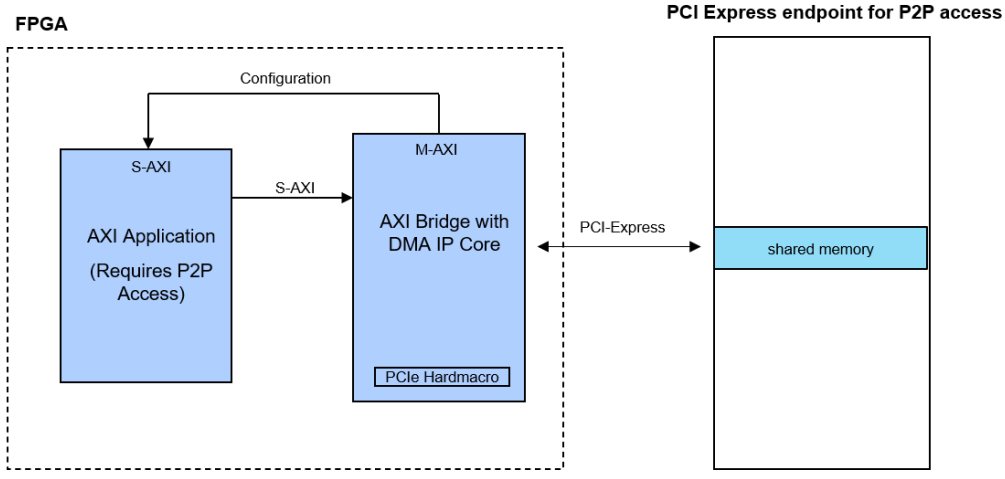
IP Application Example: “Access shared host memory”

Due to its generic architecture, the ABD IP core for PCIe fits into many applications. The following diagram shows a typical application where an AXI application requires access to a shared memory in the host memory:



IP Application Example: “Peer to Peer Communication”

Peer to Peer accesses are required, when the AXI application in the FPGA needs access to a shared memory within an other PCI Express add-in card in the same PCI Express system:



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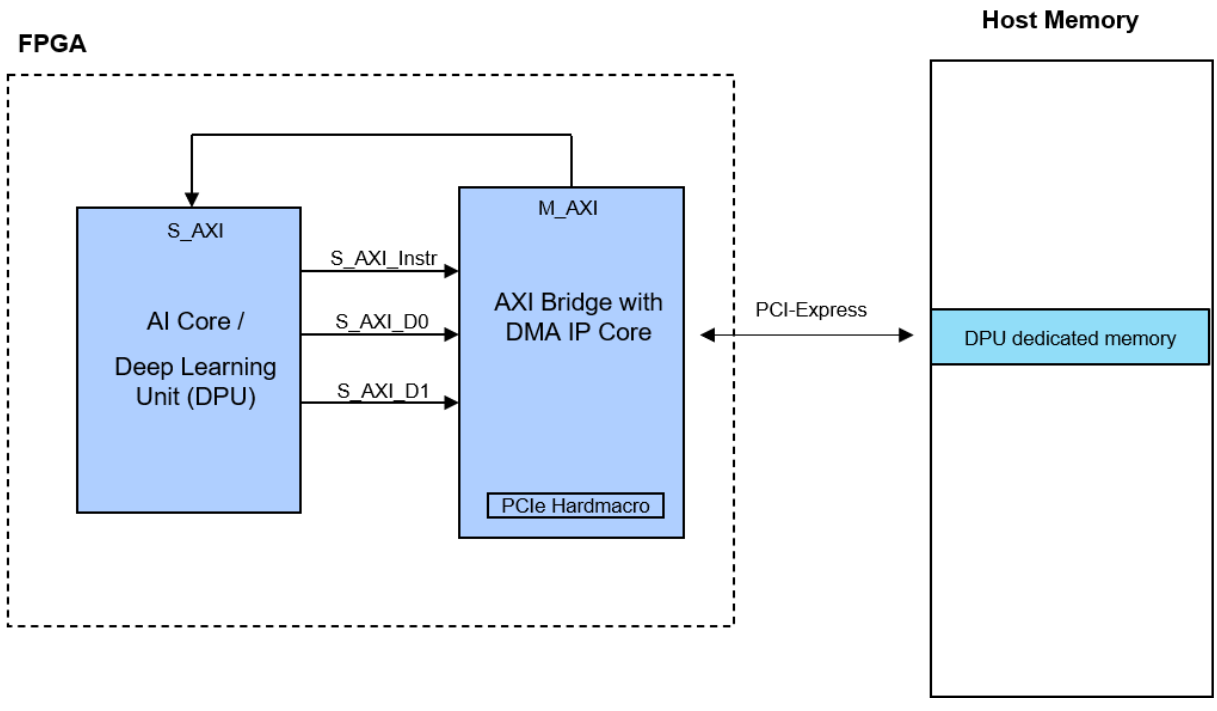
AXI Bridge Application “Deep Learning Coprocessor”

Another well-known application example is the Deep Learning Coprocessor within a FPGA, where the deep learning engine operates with memory mapped AXI interfaces. The DPU fetches the input data from Host Memory, processes it according to the implemented neural network and stores the final result in the host memory.



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FPGA Resource Utilization

The following table lists different example configurations and the required FPGA resources:

FPGA Device	Xilinx Configuration	LUTs	LUTR	FFs	BRAM
7 Series, Ultrascale Ultrascale+	256-bit Architecture, 4 S_AXI, 1 M_AXI	10,950	1,770	17,505	49,5
	Lattice Configuration	LUTs	LUTR	FFs	EBR
Certus NX	256-Bit Architecture, 1 S-AXI, 1 M-AXI				

These numbers include the resources of the PCIe Hard-IP.
LUTR are distributed RAM cells. The user can choose between BlockRAM or LUT RAM implementation style.

Deliverables

- Encrypted VHDL or source code for easy design flow integration
- Comprehensive user guide and application notes
- Reference design
- Windows or Linux driver package
- PCIe test bench with high-speed simulation mode
- Technical support

Evaluation

This IP Core can be evaluated as an encrypted version. Request a free 30-day evaluation license for ISIM, Modelsim or Aldec simulators at:

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Smartlogic is a member of the Intel Partner Alliance, Xilinx's Alliance and Lattice Partner Program.

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