DATASHEET

AXI Bridge with DMA for PCIe IP Core

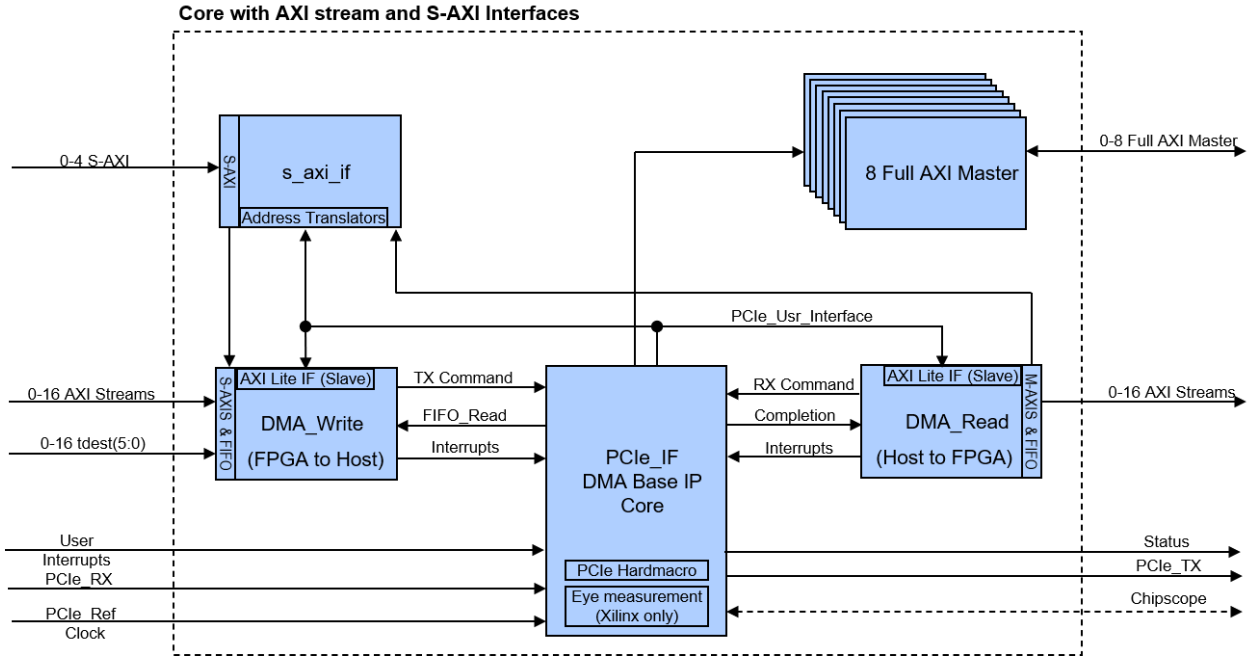
Product Overview

The AXI Bridge with DMA IP core is Smartlogic's ultimate PCIe DMA IP solution with a powerful mix of multiple industry standard AXI Interfaces. AXI Stream interfaces allow continuous data streaming from FPGA to Host or from Host to FPGA. S-AXI Memory mapped interfaces allow easy data access of remote memories in order to realize shared memory access or per to peer applications.
All interfaces support fully parallel operation without any interferences. Interfaces that are not required can be turned off individually and do not occupy logic resources.
This IP core enables the developer to build complex PCI Express endpoints with no specific PCI Express protocol know-how. The user only transmits or receives payload data and does not have to assemble valid PCI Express packets.
A powerful kernel mode device driver is shipped with the IP for Windows and Linux OS to ensure easy software integration of the core.

IP Features

- Multi-channel architecture
- Non-blocking approach, an incomplete AXI Stream packet does not block other AXI interfaces
- Up to 4 S-AXI interfaces for AXI2PCIe bridge applications (incl peer to peer applications) with up to 6 AXI BARs and dynamic address translators
- Up to 16 AXI Stream Slave interfaces
- Up to 16 AXI Stream Master interfaces
- Up to 8 AXI Masters to interface user registers
- User transmits / receives only user data without PCIe protocol knowledge
- Independent clocking and data width for each AXI interface
- Built in completion sorting: S-AXI read requests are answered always in the requested order
- Based on Xilinx / Intel / Lattice integrated PCI-Sig compliant PCIe Block (HardIP)
- Link speed Gen 1-4, link widths x1-x8
- Available for most Xilinx, Intel and Lattice devices

Block Diagram



Note : S-AXI and S-AXIS interfaces can be mixed, but the sum of interfaces must not greater than 16.

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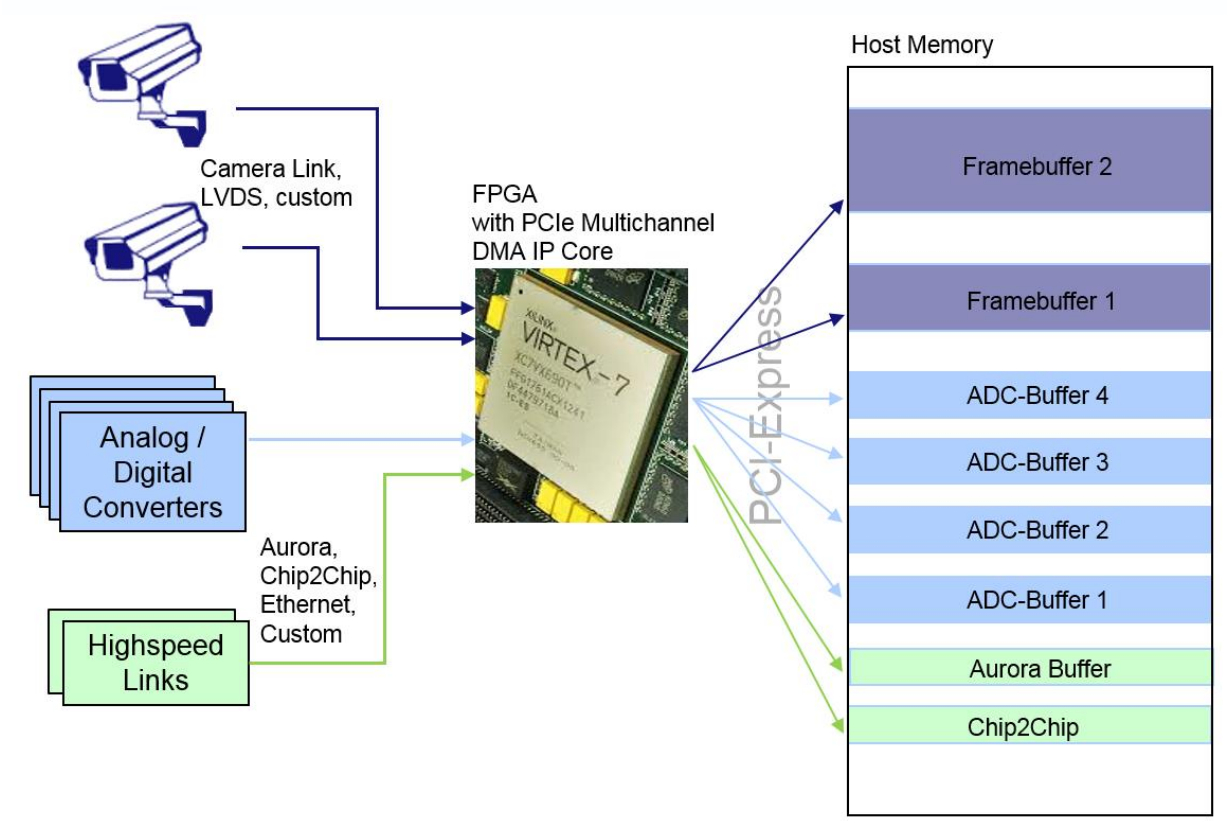
IP Application Example: “Data Streaming”

Due to its generic architecture, the ABD IP core for PCI Express fits into many applications. The following diagram shows typical streaming applications, where data streams have to be sent ordered to the host memory:



Typical streaming data sources are:

Video cameras, high-speed Analog-Digital-Converter samples, high-speed links like Aurora, Ethernet or others.

Up to 64 independent streaming sources with a dedicated target buffer are supported.

Each data interface can operate at its own clock domain and its own data width (8, 16, 32, 64, 128 or 256 Bit).

The target can be either the host memory or any other PCI Express endpoint in the system.

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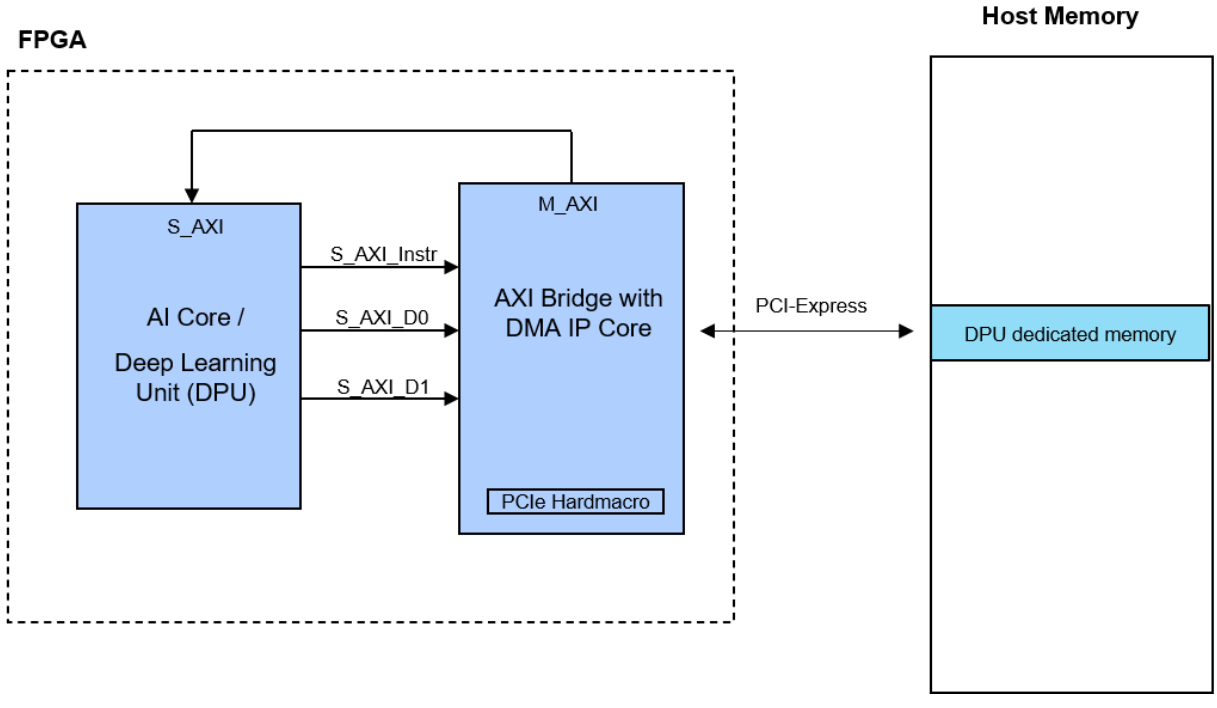
AXI Bridge Application “Deep Learning Coprocessor”

Another well-known application is the Deep Learning Coprocessor within a FPGA. The DPU fetches the input data from Host Memory, processes it according to the implemented net and stores the final result in the host memory.



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FPGA Resource Utilization

The following table lists different example configurations and the required FPGA resources:

FPGA Device	Xilinx Configuration	LUTs	LUTR	FFs	BRAM
7 Series, Ultrascale Ultrascale+	256-bit Architecture, 4 S_AXI, 1 M_AXI	10,950	1,770	17,505	49,5
	256-bit Architecture, 4 S_AXI, 4 S_AXIS, 4 M_AXIS, 1 M_AXI	15,505	3,096	25,391	87,5
	Intel Configuration	ALMs		FFs	BRAM

These numbers include the resources of the PCIe Hard-IP and the resources for the AXI Stream FIFOs for each configured channel.
LUTR are distributed RAM cells. The user can choose between BlockRAM or LUT RAM implementation style.

Deliverables

- Encrypted VHDL or source code for easy design flow integration
- Comprehensive user guide and application notes
- Reference design
- Windows or Linux driver package
- PCIe test bench with high-speed simulation mode
- Technical support

Evaluation

This IP Core can be evaluated as an encrypted version. Request a free 30-day evaluation license for ISIM, Modelsim or Aldec simulators at:

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Smartlogic is a member of the Intel Partner Alliance, Xilinx's Alliance and Lattice Partner Program.

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