DATASHEET

AXI Bridge with DMA for PCIe IP Core

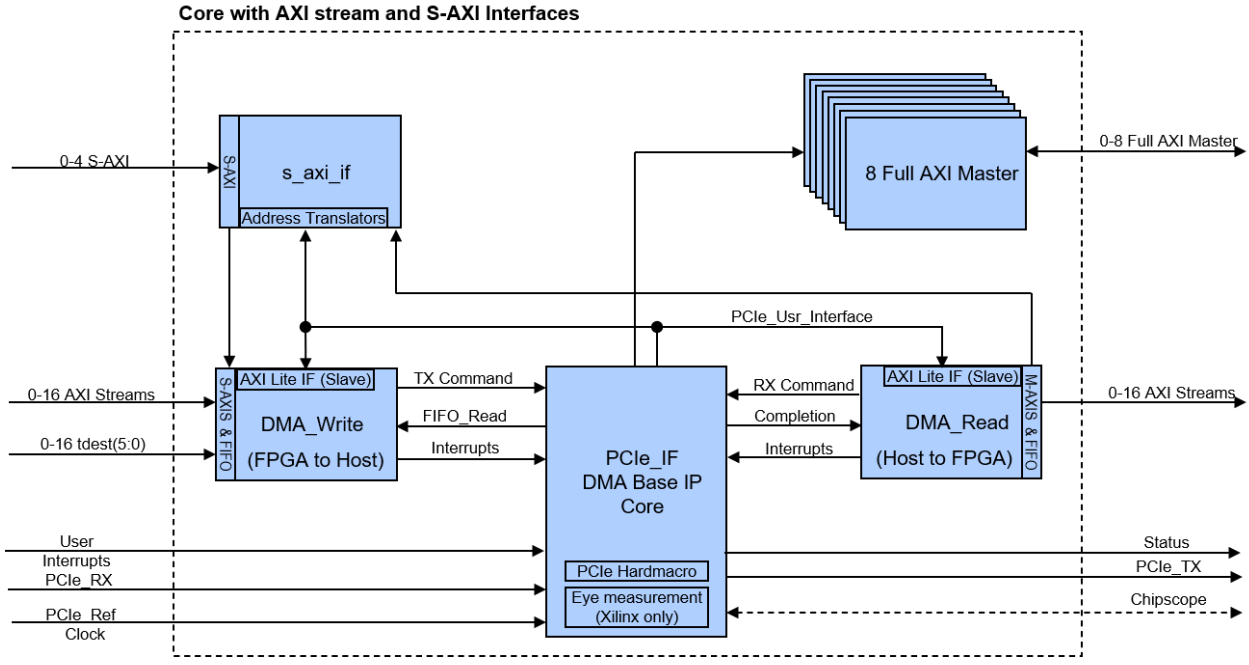
Product Overview

The AXI Bridge with DMA IP core is Smartlogic's ultimate PCIe DMA IP solution with a powerful mix of multiple industry standard AXI Interfaces. AXI Stream interfaces allow continuous data streaming from FPGA to Host or from Host to FPGA. S-AXI Memory mapped interfaces allow easy data access of remote memories in order to realize shared memory access or per to peer applications.
All interfaces support fully parallel operation without any interferences. Interfaces that are not required can be turned off individually and do not occupy logic resources.
This IP core enables the developer to build complex PCI Express endpoints with no specific PCI Express protocol know-how. The user only transmits or receives payload data and does not have to assemble valid PCI Express packets.
A powerful kernel mode device driver is shipped with the IP for Windows or Linux operating systems to ensure easy software integration of the core.

IP Features

- Lowest logic resource count in the industry
- Utilizes built-in HardFIFOs (AMD devices only)
- Multi-channel architecture
- Continuous high throughput data streaming
- Non-blocking approach, an incomplete AXI Stream packet does not block other AXI interfaces
- Up to 4 S-AXI interfaces for AXI2PCIe bridge applications (incl peer to peer applications) with up to 6 AXI BARs and dynamic address translation registers
- Up to 16 AXI Stream Slave interfaces
- Up to 16 AXI Stream Master interfaces
- Up to 8 AXI Masters to interface user registers
- User transmits / receives only user data without PCIe protocol knowledge
- Built in completion sorting: S-AXI read requests are answered always in the requested order
- Tandem, MSI and MSI-X supported
- Based on AMD / Lattice integrated PCI-Sig compliant PCIe Block (HardIP)
- Link speed Gen 1-4, link widths x1-x8

Block Diagram



Note : S-AXI and S-AXIS interfaces can be mixed, but the sum of interfaces must not greater than 16.

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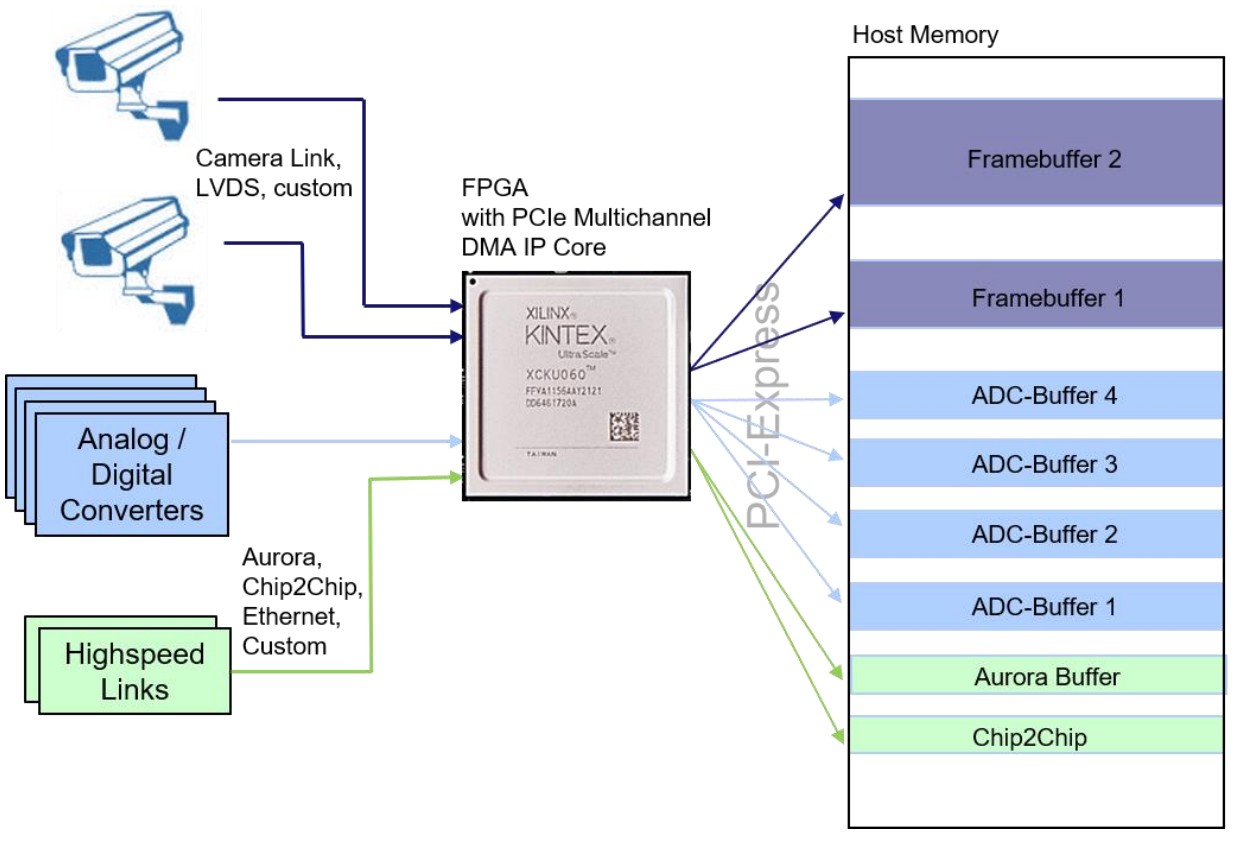
IP Application Example: “Data Streaming”

Due to its generic architecture, the ABD IP core for PCI Express fits into many applications. The following diagram shows typical streaming applications, where data streams have to be sent ordered to the host memory:



Typical streaming data sources are:

Video cameras, high-speed Analog-Digital-Converter samples, high-speed links like Aurora, Ethernet or others.

Up to 64 independent streaming sources with a dedicated target buffer are supported.

Each data interface can operate at its own clock domain and its own data width (8, 16, 32, 64, 128 or 256 Bit).

The target can be either the host memory or any other PCI Express endpoint in the system.

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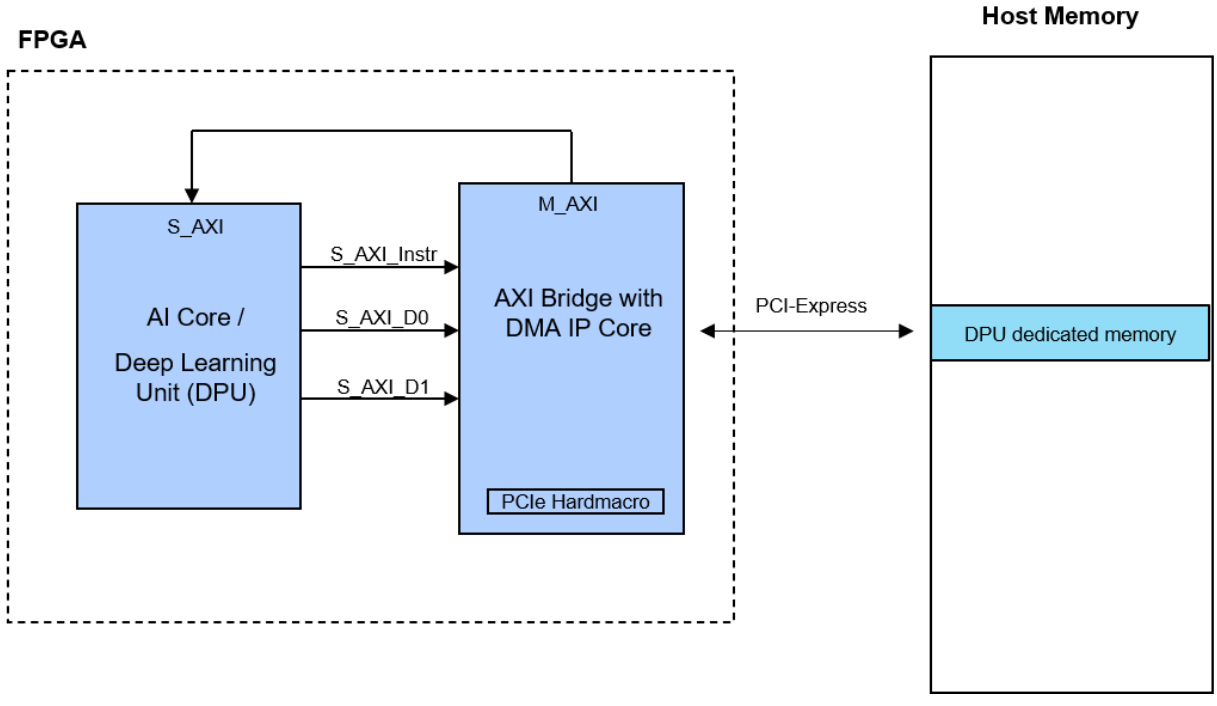
AXI Bridge Application “Deep Learning Coprocessor”

Another well-known application is the Deep Learning Coprocessor within a FPGA. The DPU fetches the input data from Host Memory, processes it according to the implemented net and stores the final result in the host memory.



Since the AXI address space is different than the PCIe address space, a dynamic address translation process is required. AXI addresses are typically fixed, whereas the PCI Express physical addresses of shared memories can change with every system boot cycle. In order to bridge the two address spaces, the IP Core has 6 dynamic address translation registers. The user mode library provides specialized API function calls to initialize these address translation registers.

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Supported FPGA Devices

The following table lists the supported FPGA vendors and FPGA device families:

FPGA Vendor	Device Family	Max PCIe Link Speed	Max PCIe Link Width
AMD	Artix-7	2	x4
	Kintex-7	2	x8
	Ultrascale	3	x8
	Ultrascale+ (Artix, Kintex, Virtex) / MPSoC	3	x8
	Versal	4	x4
		1-3	x8
	Versal Prime / Versal Gen 2	5	x2
		4	x4
		1-3	x8
	Spartan Ultrascale+	Planned for Vivado 2025.1.1	
Lattice	Certus NX Pro	3	4

FPGA Resource Utilization

The following table lists different example configurations and the required FPGA resources:

FPGA Device	AMD Configuration	LUTs	FFs	BRAM
7 Series, Ultrascale Ultrascale+, Zynq, MPSoC, Versal (PCIE4) Spartan Ultrascale+	1 S-AXIS, 0, M-AXIS, 1 M-AXI	4,156	4,738	5
	1 S-AXI, 1 M-AXI	6,376	7,672	16
	8 S-AXIS, 8 M-AXIS, 1 M-AXI	14,809	19,217	110,5

These numbers do not include the resources of the PCIe Hard-IP that is always required. The user can choose between BlockRAM or LUT RAM implementation style for most RAMs. Therefore BRAM numbers can be decreased at the cost of more LUTRAMs.

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Deliverables

- Encrypted VHDL for easy design flow integration, Source Code licensing available as option
- Comprehensive user guide and application notes
- Reference design
- Windows / Linux driver package with sophisticated user mode library
- PCIe test bench with high-speed simulation mode
- Technical support

Evaluation

This IP Core can be evaluated as an encrypted version. Request a free 30-day evaluation license for ISIM, Modelsim or Aldec simulators at:

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Smartlogic is a member of the Altera Partner Alliance, AMD's Alliance and Lattice Partner Program.

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