

# Intel IP Catalog Flow

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V 1.4



#### This AppNote describes how to use the IP catalog flow for all supported Intel FPGA devices

- How to generate the IP Core
- make specific parameter settings so that the generated IP runs with the Smartlogic core
- How to activate MSI and MSI-X interrupts (only available in the HCC version of the Smartlogic IP core)

In order to use the IP catalog flow it is necessary to reference to the correct files in the IP Database

• Make sure to use pcie\_core\_connection\_ipi.vhd instead of pcie\_core\_connection.vhd, if you are not working in multifunction mode

• In case you work with multi-function, you have to to include pcie\_core\_connection\_mf.vhd in the QSF file

• In case you migrate from the old flow to the new IP catalog flow, you have to delete the direct references to the Intel HIP related files. By adding the HIP IP core from the IP catalog, these files will be added automatically again in the background via the .ip / .qip files.

• A demo project is available that works as an example

For Cyclone V FPGAs two IP catalog cores have to be generated and added to the design:

- 1. The Transceiver Reconfiguration Controller Intel FPGA IP core with the IP variation filename "transceiver\_reconfig.v"
- 2. The "Cyclone V Hard IP for PCI Express Intel FPGA" IP core with the IP variation filename "intel\_c5\_pcie2.v"

Select those IPs in the IP catalog and prepare them for configuration by double clicking. Make sure that your project contains the following flow specific files:

• The file "pcie\_core\_connection\_ipi.vhd" has to be added to the project instead of pcie\_core\_connection.vhd in non multi function mode and pcie\_core\_connection\_mf.vhd in multi function mode.

• The IP Core wrapper File "altera\_a5\_c5\_pcie2\_wrapper.v" has to be added to the project instead of the file "altera\_c5\_pcie2.sv"

#### GUI of the Transceiver Reconfiguration Controller

🔨 Transceiver Reconfiguration Controller Intel FPGA IP - transceiv	er_reconfig	– 🗆 X	(
Transceiver Reconfiguration Control alt_xcvr_reconfig	ler Intel FPGA IP	<u>D</u> ocumentation	
👻 Block Diagram	▼ Parameters		
Show signals	Cyclone V     Cyclone V	nd transceiver PHY.	
	The Analog Features		- Internet
	Enable Analog controls		
	Reconfiguration Features		- Internet
	Enable channel/PLL reconfiguration		A CONTRACT
	Enable PLL reconfiguration support block		annan annan anna
<ul> <li>Info: transceiver_reconfig: reconfig_from_xcvr port width is 5</li> <li>Info: transceiver_reconfig: reconfig_to_xcvr port width is 5*70</li> </ul>	*46 bits ) bits		
	EDA Options	Cancel Finish	

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Special care has to be taken regarding the number of reconfiguration interfaces and the duty cycle correction. The next two slides show how to configure them correctly.

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Duty cycle correction : Working around a Quartus Prime GUI Problem

First check "Enable duty cycle calibration" and the GUI should look like this:



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Now deselect Enable duty cycle calibration, while leaving "Calibrate duty cycle during power up" checked and the GUI looks like this :



Although it seems, that no duty cycle calibration is selected, the "Calibrate duty cycle during power up" is still active. This is the correct setting.

The number of reconfiguration interfaces has to be entered according to the following table:

PCIe Linkwidth	Number of reconfiguration interfaces
X1	2
X2	3
X4	5

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### Cyclone V – Transceiver Reconfiguration Controller



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After you have generated the Transceiver Reconfiguration Controller, open the generated file "transceiver\_reconfig.v" with a text editor. The parameter settings of alt\_xcvr\_reconfig .enable\_dcd must be 0 and .enable\_dcd\_power\_up, .enable\_offset and .enable\_analog must be 1. If they have a different setting, repeat the configuration process for the IP.

### Cyclone V – Configuring the HIP

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### GUI of the Cyclone V HIP:

ock Diagram	▼ System Settings	
intel_c5_pcie2  r conduit clock conduit clik clock conduit clock conduit clock conduit	Number of lanes:       x4 y         Lane rate:       Gen2 (5.0 Gbps) v         Port type:       Native endpoint v         Application interface:       Avalor-ST 128-bit v         RX buffer credit allocation - performance for received requests:       Gwv v         Reference clock frequency:       100 MHz v         Use 62.5 MHz application clock       100 MHz v         Use deprecated RX Avalon-ST data byte enable port (rx_st_be)       Enable configuration via the PCIe link         Enable configuration       Number of Functions:         v       function Capabilities         v       Shared PCI Express/PCI Capabilities Across All Functions         Device       Error Reporting         Link       Slot clock configuration         Vink port number:       1         v       Slot clock configuration	
o: intel_c5_pcie2: Cyclone V Hard IP for PCI Express Inte o: intel_c5_pcie2: Device family is Cyclone V o: intel_c5_pcie2: Gen2x4 support available only for GT I o: intel_c5_pcie2: The application clock frequency (pld_c o: intel_c5_pcie2: 5 reconfiguration interfaces are requir o: intel_c5_pcie2: Credit allocation in the 6K bytes receiv o: intel_c5_pcie2: Posted : header=16 data=16	IFPGA IP v19.1 Devices dk) is 125 Mhz ed for connection to the external reconfiguration controller e buffer:	

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GUI of the Cyclone V HIP : Example how to activate 32 MSI-X interrupts :

X Cyclone V Hard IP for PCI Express Intel FPGA IP - intel_c5_pcie2	- 0	×
Cyclone V Hard IP for PCI Express Intel FPGA IP altera_pcie_cv_hip_ast	<u>D</u> ocume	ntation
Block Diagram       Device ID:       0x0000001         Show signals       Device ID:       0x0000000         Class Code:       0x0000000         Class Code:       0x0000001         Subsystem Vendor ID:       0x0000001         bip_ctrl       conduit       corecilout, hip         pid_cik       clock       avalon_streaming       rx_st         ts_st       avalon_streaming       rx_st       31         ts_rered       conduit       conduit       recorfig_to xxvr,         ts_rered       conduit       conduit       conduit         ip_j rst       conduit       conduit       conduit         recorfig_to xxvr,       rable offset       16384         ts_rered       conduit       conduit       conduit         conduit       conduit       conduit       conduit         rable BAR indicator:       0       Pending bit array (PBA) offset       1922         PBA BAR Indicator:       0       PBA BAR Indicator:       0		
<ul> <li>Info: intel_c5_pcie2: Cyclone V Hard IP for PCI Express Intel FPGA IP v19.1</li> <li>Info: intel_c5_pcie2: Device family is Cyclone V</li> <li>Info: intel_c5_pcie2: Gen2x4 support available only for GT Devices</li> <li>Info: intel_c5_pcie2: The application clock frequency (pld_clk) is 125 Mhz</li> <li>Info: intel_c5_pcie2: 5 reconfiguration interfaces are required for connection to the external reconfiguration controller</li> <li>Info: intel_c5_pcie2: Credit allocation in the 6K bytes receive buffer:</li> </ul>	Cancel	Finish

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Currently only 32 MSI-X interrupts are supported, please do not try to enter other values.

Also make sure to set the generic/parameter use\_msix\_g to 1 !

It has been observed for Cyclone V, that the GUI parameters might not be transferred correctly to the IP's HDL parameter section during the IP generation process of Quartus. This problem happens especially when the link speed is changed form Gen2 to Gen1. In this case the GUI looks right, but the 62.5 MHz option is activated in error. This results in an illegal PCIe HIP configuration and the FPGA design does not communicate correctly via PCIe and causes a system crash.

A clear indication that your design is affected is when Quartus reports warning message #332056.

Example:

<ul> <li>System Settings</li> </ul>	
Number of lanes:	x4 🗸
Lane rate:	Gen1 (2.5 Gbps) 🔽
Port type:	Native endpoint 🔽
Application interface:	Avalon-ST 64-bit 🔽
RX buffer credit allocation - performance for received requests:	Low
Reference clock frequency:	100 MHz 🗸
Use 62.5 MHz application clock	
Use deprecated RX Avalon-ST data byte enable port (rx_st_t	pe)
Enable configuration via the PCIe link	
Enable Hard IP reconfiguration	
Number of Functions:	1 🗸

Although "use 62.5 MHz application clock" is unchecked, the generated IP might have this option turned on.

In order to check, if your design is affected, open the generated file intel\_c5\_pcie2.v and search for the parameter .enable\_adapter\_half\_rate\_mode\_hwtcl:

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If this parameter is set to "true" and you are not operating in G2-X4 mode, your design is affected.

In this case you have to set all 4 checkboxes in the "System Settings" Tab (see previous page) and then clear them all and re-generate the IP again. Do not change the verilog file as it will be overwritten when you change other parameters. After re-generating the file, re-check if the setting of enable\_adapter\_half\_rate\_mode\_hwtcl is now correct.

Summary of the Quartus GUI Error:

- The GUI error seems to affect all IP cores
- Problem is, that the GUI representation of the checkboxes seems not to be in sync with the real parameter values

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- This problem leads to illegal designs and even system crashes
- It has been observed in QuartusPrime Lite 19.1 and might occur also in newer versions
- Most likely it affects not only Cyclone V but also all other FPGA design families

#### Important when you configure the Cyclone V HIP core:

- Never check "Use 62.5 MHz application clock". The Smartlogic IP will not work with this setting
- Never check "use rx\_st\_be"
- Set the RX Buffer credit allocation to "Low" when the FPGA uses DMA Read. In all other cases, set this to "Balanced"
- You may turn on "Enable configuration via the PCIe link" also known as CVP If you turn on CVP make sure, that the PCIe 100 MHz reference clock is connected to sys\_clk\_ip of the Smartlogic IP core and that a free running 125 MHz clock is connected to sys\_clk\_in of the Smartlogic IP core. If you do not work with CVP, connect the 100 MHz clock to both sys\_clk\_ip and sys\_clk\_in
- Check "slot clock configuration", if you are operating with a common reference clock between root complex and FPGA endpoint
- If you are running in Gen2-X4 mode, make sure to set the Application interface to Avalon-ST 128-Bit. In all other cases use the 64-Bit version
- Set the Device Identification Registers and the PCI Express Capabilities for Func 0 according to your needs
- You may configure additional PCIe functions in case you have a multi-function license

A demo design, where the Cyclone V IPs are correctly setup, is available from Smartlogic.

Make sure to configure the following parameters of the Smartlogic IP core in the same way as you entered them into the HIP GUI:

pcie\_ep\_config\_pkg.vhd

Parameter	Comment
PCle_synth_Core_Type_c	"CV"
Enable_SLOT_CLOCK_C	
PCIE_MSI_CAP_MULTIMSGCAP_C	
PCIe_BAR <x>_C</x>	
PCIe_CLASS_CODE_C	
PCIe_VEN_ID_C	Set these constants in the same way as you
PCIe_DEV_ID_C	entered them in the GUI.
PCIe_SUBSYS_VEN_ID_C	
PCIe_SUBSYS_DEV_ID_C	
PCle_link_cap_max_link_speed_c	
PCle_link_cap_max_link_width_c	

The Avalon ST data bitwidth has to be entered according to the following table:

PCIe Linkspeed / Linkwidth	Avalon ST bitwidth
G2-X4	128
G1-X8	128
All other link width / link speed combinations	64

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For Arria 10 FPGAs one IP catalog core has to be generated and added to the design:

1. The "Arria 10 Hard IP for PCI Express" IP core with the IP variation filename "altera\_a10\_pcie3.v"

Make sure that your project contains the following flow specific files:

• The file "pcie\_core\_connection\_ipi.vhd" has to be added to the project instead of pcie\_core\_connection.vhd. Note that PCIe multi-function is not supported from the PCIe HIP for Arria 10.

• The IP Core wrapper File "altera\_a10\_pcie3\_wrapper.v" has to be added to the project

### Arria 10 – Configuring the HIP

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#### GUI of the Arria 10 HIP:

🔓 IP Parameter Editor Pro - altera_a10_pcie3 (D:\PCle_IP\Altera\QuartusPrime_HCC_Demo_256\DMA_Demo3_Arria_X\Local_IP\altera_a10_pcie3.ip) — 🗌 🗙			
<u>Eile Edit System Generate View T</u> ools <u>H</u> elp			
System: altera a10 prie3. Path: prie a10 bin 0.	Details 🛛 👑 Block Symbol 🖾 🗕 🗗		
Intel Arria 10/Cyclone 10 Hard IP for PCI Express altera_pcie_a10_hip Generate Example Design	✓ Show signals     pcie_a10_hip_0		
Design Environment         This component supports multiple interface views:         Standalone         IP Settings       Example Designs         PCI Express / PCI Capabilities       Configuration, Debug and Extension Options       PHY Characteristics         System Settings       Avalon-ST Settings       Base Address Registers       Device Identification Registers         Application interface type:       Avalon-ST <ul> <li>Gen2:x4, Interface: 128 bit, 125 MHz</li> <li>Port type:</li> <li>RX buffer credit allocation for received requests vs completions:</li> <li>Low</li> <li>RX Buffer completion credits:</li> <li>Header: 195 Data:773</li> </ul>	2       pld_clk       coreclk         pld_clk       ck       ck         refclk       ck       startofpacket         npor       endofpacket       endofpacket         pin_perst       pin_perst       ready         pld_clk_inuse       pld_core_ready       empty         gd_clk_inuse       pld_ck_inuse       pld_clr_st         gerdes_pil_ocked       serdes_pil_ocked       reset         reset       estatus       reset         Presets       2		
	Project Click New to create a preset. Library		
	No presets for Intel Arria 10/Cyclone 10 Hard IP for PCI Expre		
👌 System Messages 🔅 🗕 – 🗗 D			
Type Path Message			
Altera a10 ncia3 ncia a10 hin 0 device family is ária 10	-		
altera a10 pcie3.pcie_a10_inp_0 device_rammins Anna 10			
altera a10 pcie3.pcie a10 hip 0 Gen2 (5.0 Gbps) x4 128-bit			
	Apply Update Delete New		
0 Errors, 0 Warnings	Generate HDL		

### Arria 10 – Configuring the HIP

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#### GUI of the Arria 10 HIP:

🐇 IP Parameter Editor Pro - altera_a10_pcie3* (D:\PCIe_IP\Altera\QuartusPrime_HCC_Demo_256\DMA_Demo2_qpp\Local_IP\altera_a10_pcie3.ip) — 🗆 X			
Eile Edit System Generate View Tools Help			
N Parameters 🕱 – 🗗 🗖	Details 🛛 💾 Bloc 😂 💶 🗗 🗖		
System: altera_a10_pcie3 Path: pcie_a10_hip_0	Chevy eignele		
Details	Show signals		
altera prica a10 hip	pcie		
	pid cik		
Design Environment	pid_cik		
This components supports manaple menace views.	refcik —		
Standatorie	clk		
IP Settings / Example Designs	npor		
(PCI Express / PCI Carabilities ) Configuration Debug and Extension Options / PEV Characteristics	pin_perst pin_perst		
System Settings Avaion-ST settings Base Address Registers Device Identification Registers	hip_rst		
Fi Enable Avalon-ST Reset output port	pld_core_ready pld_core_rea		
Enable byte parity ports on Avalon-ST interface	serdes_pll_lockedserdes_pll_l		
Enable multiple packets per cycle for the 256-bit interface	reset_status reset_status		
Enable credit consumed selection port	hip_ctrl		
Enable Configuration Bypass (CfdBP)	test_in[310] test_in		
Enable local management interface (LMI)	simu_mode_pipesimu_mode_		
	derr_cor_ext_rcv		
	derr_cor_ext_rpl derr_cor_ext		
	derr_rpi diup		
	dup_exit dup_exit		
🚰 System Messages 🛛 – 🗗 🗖	ev128ns ev1us ev1us		
Type Path Message	hotrst_exit hotrst_exit		
Y 🔺 2 Warnings	12_exit 12_exit		
A altera_a10_pcie3.pcie_a10_hip_0.tx_st The empty signal width should be 1 bits.	lane_act[30] lane_act		
A altera_a10_pcie3.pcie_a10_hip_0.rx_st The empty signal width should be 1 bits.	rx_par_err		
Y     3 Into Messages	tx_par_err[10] tx_par_err		
🔓 Presets 🛱 🗗			
0 Errors, 2 Warnings	Generate HDL		

Enable only the Avalon-ST Reset output port. Never turn on "Enable multipackets per cycle for the 256-Bit Interface"

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#### Important when you configure the Arria 10 HIP core:

• Set the RX Buffer credit allocation to "Low" when the FPGA uses DMA Read. In all other cases, set this to "Balanced"

• You may turn on "Enable configuration via the PCIe link" also known as CVP

If you turn on CVP make sure, that the PCIe 100 MHz reference clock is connected to sys\_clk\_ip of the Smartlogic IP core and that a free running 125 MHz clock is connected to sys\_clk\_in of the Smartlogic IP core. If you do not work with CVP, connect the 100 MHz clock to both sys\_clk\_ip and sys\_clk\_in

- For Signal Integrity measurements, you may turn on ADME to use the transceiver toolkit
- Check "slot clock configuration", if you are operating with a common reference clock between root complex and FPGA endpoint
- Set the Device "Identification Registers" and the "Base Address Registers" according to your needs
- Choose "maximum payload size" according to the capabilities of your root complex
- The Arria 10 PCIe HardIP does not support PCIe multi-function

A demo design, where the Arria 10 HIP is correctly setup is available from Smartlogic.

Make sure to configure the following parameters of the Smartlogic IP core in the same way as you entered them into the HIP GUI:

pcie\_ep\_config\_pkg.vhd

Parameter	Comment
PCIe_synth_Core_Type_c	"АХ"
Enable_SLOT_CLOCK_C	
PCIE_MSI_CAP_MULTIMSGCAP_C	
PCIe_BAR <x>_C</x>	
PCIe_CLASS_CODE_C	
PCIe_VEN_ID_C	Set these constants in the same way as you
PCIe_DEV_ID_C	entered them in the GUI.
PCIe_SUBSYS_VEN_ID_C	
PCIe_SUBSYS_DEV_ID_C	
PCle_link_cap_max_link_speed_c	
PCle_link_cap_max_link_width_c	

The Avalon ST data bitwidth has to be entered according to the following table:

PCIe link speed / link width	Avalon ST bit width
G3-X8, G3-X4, G2-X8	256
G1-X8, G2-X4, G3-X2	128
G1-X1, G1-X2, G1-X4, G2-X1, G2-X2, G3-X1	64

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#### GUI of the Arria 10 HIP : Example how to activate 32 MSI-X interrupts :

File Edit System Generate View Tools Help	(coca_n (arch_aro_percomp)		
The first Global Source Tesh			
N Parameters 💥	-	Details 💥 🎽 Block Symbol 💥 📃 🚽 🗗	
System: altera_a10_pole3 Path: pole_a10_hip_0		Show signals	
Intel Arria 10/Cyclone 10 Hard IP for PCI Express			
altera_pcie_a10_hip	Generate Example Design	pcie_a10_hip_0	
Design Environment	<u> </u>	pid_cik, corecik	
This component supports multiple interface views:		pld_clk clk	
Standalone		refcik rx_st	
		clk startofpacket	
IP Settings Example Designs		porerror	
PCI Express / PCI Canabilities Configuration Debug and Extension Options PHY Characteristics		pin_perst valid	
System Settings Avalon-ST Settings Base Address Registers	Device Identification Registers	hip_rst data	
Device / Error Reporting / Link / MSI / MSI-X / Slot / Power Management / VSEC	_	pld_core_readypld_core_readypld_core_ready	
		serdes_pll_locked serdes pll locked cir_st	
Table size:		reset_status reset	
Table offset 31			
Table Oriset		🐻 Presets 🛛 🗕 🗗	
Pending bit array (PBA) offset 0x00002000		Presets for pcie_a10_hip_0	
PBA BAR Indicator: 0		Clear preset filters	
		Project	
		Click New to create a preset.	
	•	Library - No presets for Intel Arria 10/Cyclone 10 Hard IP for PCI Expre	
AE System Messages 🛞	_ ಗೆ 🗆		
Type Path Message			
9 () 3 Info Messages			
Image:			
Image:			
Image:			
		Apply Update Delete New	
0 Errors, 0 Warnings		Generate HDL.	

Currently only 32 MSI-X interrupts are supported, please do not try to enter other values.

Also make sure to set the generic/parameter use\_msix\_g to 1 !

For Stratix 10 FPGAs one IP catalog core has to be generated and added to the design:

1. The "Avalon-ST Intel Stratix 10 Hard IP for PCI Express" IP core with the IP variation filename "altera\_S10\_pcie3.v"

Make sure that your project contains the following flow specific files:

- The file "pcie\_core\_connection\_ipi.vhd" has to be added to the project instead of pcie\_core\_connection.vhd
- The IP Core wrapper File "altera\_s10\_pcie3\_wrapper.v" has to be added to the project

### Stratix 10 – Configuring the HIP

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#### GUI of the Stratix 10 HIP:

LP Parameter Editor Pro - altera_S10_pcie3 (D:\PCIe_IP\A	Altera\QuartusPrime_HCC_Demo_256\DM	A_Demo2_qpp\Local_IP_S10\altera_S1	0_pcie3.ip) — □ ×			
<u>File E</u> dit <u>S</u> ystem <u>G</u> enerate <u>V</u> iew <u>T</u> ools <u>H</u> elp						
🖄 Parameters 🛞 🛛 📑 🖬 🚯 Details 🕺 Block Symbol 🕮 💶 🖻						
System: altera_S10_pcie3 Path: altera_S10_pcie3						
Avaion-ST Intel Stratix 10 Hard IP for PCI Express altera_pcie_s10_hip_ast         Details           Generate Example Design			Avalon-ST Intel Stratix			
Design Environment This component supports multiple interface views:			Express			
System	Name					
			Version			
IP Settings Example Designs			Author			
PCI Express / PCI Capabilities Configuration, Debug and Extension Options PHY Characteristics			Description			
System Settings Avalon-ST Settings	Base Address Registers Devic	ce Identification Registers	Crown			
Device Link MSI MSI-X Slot Power N	Device Link MSI MSI-X Slot Power Management VSEC					
Maximum payload size supported: 512 Bytes 💌						
✓ PF0 Support Extended Tag Field						
✓ Function level reset			🍯 Presets 🕴 🗕 🗗 🗖			
			Presets for altera_S10_pcie3			
			Clear preset filters			
			×			
			Project			
			Click New to create a preset.			
			No presets for Avalon-ST Intel Stratix 10 Hard IP for I			
or a strange and a strange an		- =				
Type Path	Mess	age				
P 🛕 1 Warning						
Altera_\$10_pcie3.altera_\$10_pcie3.rx_st	t The empty signal width should be 1 bit	5.				
9 🕕 1 Info Message						
altera_\$10_pcie3.altera_\$10_pcie3	Gen3 (8.0 Gbps) x8 256-bit					
			Apply Update Delete New			
0 Errors, 1 Warning			Generate HDL			

#### Important when you configure the Stratix 10 HIP core:

• You may turn on "Enable configuration via the PCIe link" also known as CVP

If you turn on CVP make sure, that the PCIe 100 MHz reference clock is connected to sys\_clk\_ip of the Smartlogic IP core and that a free running 125 MHz clock is connected to sys\_clk\_in of the Smartlogic IP core. If you do not work with CVP, connect the 100 MHz clock to both sys\_clk\_ip and sys\_clk\_in

- For Signal Integrity measurements, you may turn on ADME to use the transceiver toolkit
- Check "slot clock configuration", if you are operating with a common reference clock between root complex and FPGA endpoint
- Set the Device "Identification Registers" and the "Base Address Registers" according to your needs
- Choose "maximum payload size" according to the capabilities of your root complex
- In case you are working with DMA Read you can check the "PF0 Support Extended Tag Field" to improve performance. However this uses more BRAM resources
- multifunction is only supported for Stratix H-Tile devices

A Demodesign, where the Stratix 10 HIP is correctly setup is available from Smartlogic as a reference.

The Avalon ST data bit width has to be entered according to the following table:

PCIe Linkspeed / Linkwidth	Avalon ST bitwidth		
G3-X8, G3-X4, G2-X8, G2-X16	256		
G1-X8, G2-X4, G3-X2	128		
G1-X1, G1-X2, G1-X4, G2-X1, G2-X2, G3-X1	64		

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GUI of the Stratix 10 HIP : Example how to activate 32 MSI-X interrupts :

IP Parameter Editor Pro - altera_S10_pcie3* (D:\PCle_IP\ ile <u>E</u> dit <u>System</u> <u>Generate</u> <u>View</u> <u>T</u> ools <u>H</u> elp	Altera\QuartusPrime_HCC_Demo_256\DI	VA_Demo2_qpp\Local_IP_S10\altera_S1	0_pcie3.ip)	-		
Network Control Party Party Control Co	🔋 Details 🛛 Block Symbol 🖾 🗕 🗗					
System:         altera_S10_poile3         Path:         altera_S10_poile3           Avaion-ST Intel Stratix 10 Hard IP for PCI Express         Details           altera_poile_s10_hip_ast         Generate Example Design			IP Settings			
Design Environment This component supports multiple interface views: System			System Settings     Application Selects either the     interface Avalon Streaming or     time Avalon Streaming or			
IP Settings         Example Designs           PCI Express / PCI Capabilities         Configuration, Debug and Extension Options         PHY Characteristics			Hard IP Mode	interface Selects the width of the data interface	,	
System Settings         Avalon-ST Settings         Base Address Registers         Device Identification Registers           Device         Link         MSI         MSI-X         Slot         Power Management         VSEC           PF0 MSI-X				between the transaction laver ar		
Image: Construction         31           Table offset:         0x00000000000000000000000000000000000			Presets 83 d* c			
Table BAR indicator:         0           Pending bit array (PBA) offset:         0x00000000000000000000000000000000000						
			Project Click New to cru Library No presets for An	eate a preset. valon-ST Intel Stratix 10	Hard IP fo	
ŏ≣ System Messages 🛛 🕅		- 🗗 🗖				
Type Path	Mess	age				
ې 🔬 1 Warning						
altera_\$10_pcie3.altera_\$10_pcie3.rx_s	t The empty signal width should be 1 bi					
Y      Into Message						
<pre>up attera_\$10_pcie3.altera_\$10_pcie3</pre>	Gen3 (8.0 Gbps) x8 256-bit		Apply Upd	ate Delete	New	
0 Errors, 1 Warning				Ge	nerate HDL	

Currently only 32 MSI-X interrupts are supported, please do not try to enter other values.

Also make sure to set the generic/parameter use\_msix\_g to 1 !

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Make sure to configure the following parameters of the Smartlogic IP core in the same way as you entered them into the HIP GUI:

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pcie\_ep\_config\_pkg.vhd

Parameter	Comment		
PCIe_synth_Core_Type_c	"SX"		
Enable_SLOT_CLOCK_C			
PCIE_MSI_CAP_MULTIMSGCAP_C			
PCIe_BAR <x>_C</x>			
PCIe_CLASS_CODE_C			
PCIe_VEN_ID_C	Set these constants in the same way as you		
PCIe_DEV_ID_C	entered them in the GUI.		
PCIe_SUBSYS_VEN_ID_C			
PCIe_SUBSYS_DEV_ID_C			
PCle_link_cap_max_link_speed_c			
PCle_link_cap_max_link_width_c			